




# Power MOSFETS


## DATASHEET

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**LM123NEI3A**

N-Channel  
Enhancement Mode MOSFET

 Leadpower-semiconductor Corp., Ltd

 sales@leadpower-semi.com

 (03) 6577339 FAX : (03) 6577229

 www.leadpower-semi.com

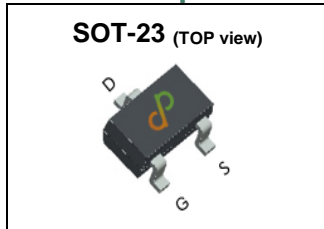


Quality Management Systems

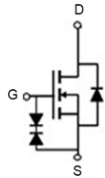
ISO 9001:2015 Certificate

## N-Channel Enhancement Mode MOSFET

### Pin Description



### Symbol



### Product Summary

Symbol	N-Channel	Unit
$V_{DSS}$	100	V
$R_{DS(ON)-Max}$	6	$\Omega$
$I_D$	0.21	A

### Feature

- Extremely low threshold voltage
- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- ESD Protection

### Applications

- Portable Equipment

### Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM123NEI3A	SOT-23	Tape & Reel	10000 / Tape & Reel	28□□□

### Absolute Maximum Ratings (T<sub>J</sub>=25°C Unless Otherwise Noted)

Symbol	Parameter	N-Channel	Unit	
$V_{DSS}$	Drain-Source Voltage	100	V	
$V_{GSS}$	Gate-Source Voltage	±20		
$T_J$	Maximum Junction Temperature	150	°C	
$T_{STG}$	Storage Temperature Range	-55 to 150	°C	
$I_{DM}^{①}$	Pulse Drain Current Tested	$T_A=25^\circ C$	0.5	A
$I_D$	Continuous Drain Current	$T_A=25^\circ C$	0.21	A
		$T_A=70^\circ C$	0.17	
$P_D$	Maximum Power Dissipation	$T_A=25^\circ C$	0.5	W
		$T_A=70^\circ C$	0.3	

### Thermal Characteristics

Symbol	Parameter	Rating	Unit	
$R_{\theta JA}^{②}$	Thermal Resistance-Junction to Ambient	Steady State	250	°C/W

Note ① : Max. current is limited by junction temperature.

Note ② : Surface Mounted on 1in<sup>2</sup> FR-4 board with 1oz.

## N-Channel Electrical Characteristics (T<sub>J</sub>=25°C Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static Electrical Characteristics</b>						
<b>BV<sub>DSS</sub></b>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>DS</sub> =250uA	100	-	-	V
<b>I<sub>DSS</sub></b>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =80V, V <sub>GS</sub> =0V	-	-	1	uA
<b>V<sub>GS(th)</sub></b>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>DS</sub> =250uA	1.5	-	2.5	V
<b>I<sub>GSS</sub></b>	Gate Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±10	uA
<b>R<sub>DS(ON)</sub></b> <sup>③</sup>	Drain-Source On-state Resistance	V <sub>GS</sub> =10V, I <sub>DS</sub> =0.2A	-	-	6	Ω
		V <sub>GS</sub> =4.5V, I <sub>DS</sub> =0.15A	-	-	9	
<b>Dynamic Characteristics</b> <sup>④</sup>						
<b>R<sub>G</sub></b>	Gate Resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, Freq.=1MHz	-	150	-	Ω
<b>C<sub>iss</sub></b>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =25V, Freq.=1MHz	-	40	-	pF
<b>C<sub>oss</sub></b>	Output Capacitance		-	5	-	
<b>C<sub>rss</sub></b>	Reverse Transfer Capacitance		-	3	-	
<b>t<sub>d(ON)</sub></b>	Turn-on Delay Time	V <sub>GS</sub> =10V, V <sub>DS</sub> =30V, I <sub>D</sub> =0.2A, R <sub>GEN</sub> =6Ω	-	3.4	-	nS
<b>t<sub>r</sub></b>	Turn-on Rise Time		-	19	-	
<b>t<sub>d(OFF)</sub></b>	Turn-off Delay Time		-	8.2	-	
<b>t<sub>f</sub></b>	Turn-off Fall Time		-	20	-	
<b>Q<sub>g</sub></b>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =30V, I <sub>D</sub> =0.2A	-	1.8	-	nC
<b>Q<sub>gs</sub></b>	Gate-Source Charge		-	0.4	-	
<b>Q<sub>gd</sub></b>	Gate-Drain Charge		-	0.3	-	
<b>Source-Drain Characteristics</b>						
<b>V<sub>SD</sub></b> <sup>④</sup>	Diode Forward Voltage	I <sub>SD</sub> =0.2A, V <sub>GS</sub> =0V	-	0.8	1.3	V
<b>t<sub>rr</sub></b>	Reverse Recovery Time	I <sub>F</sub> =0.2A,	-	36	-	nS
<b>Q<sub>rr</sub></b>	Reverse Recovery Charge	dI <sub>F</sub> /dt=100A/μs	-	35	-	nC

Note ③ : Pulse test (pulse width≤300us, duty cycle≤2%).

Note ④ : Guaranteed by design, not subject to production testing.

## N-Channel Typical Characteristics

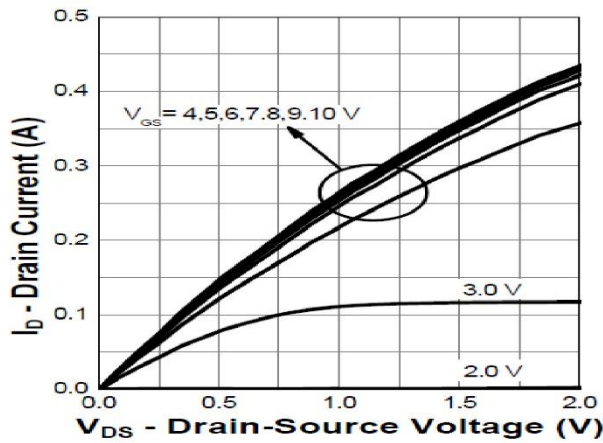


Figure 1. Output Characteristics

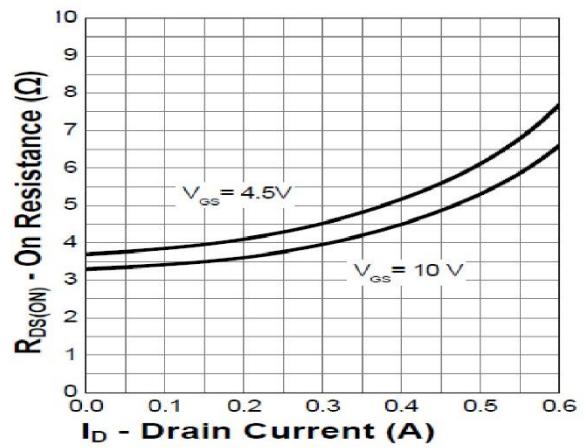


Figure 2. On-Resistance vs.  $I_D$

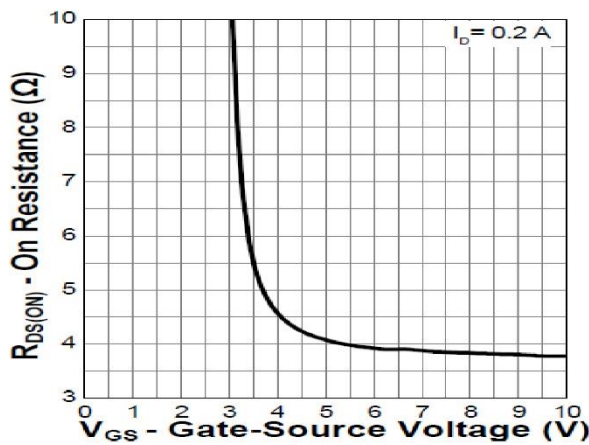


Figure 3. On-Resistance vs.  $V_{GS}$

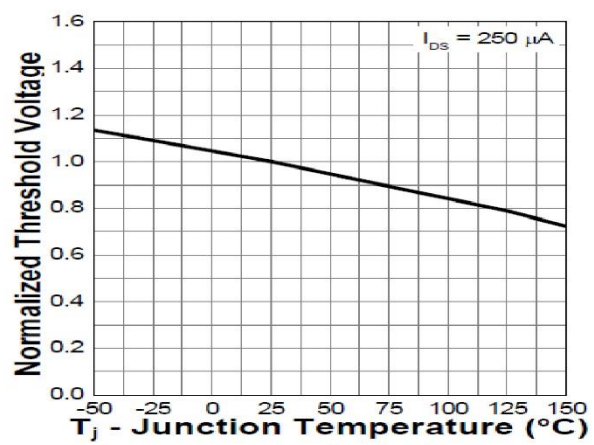


Figure 4. Gate Threshold Voltage

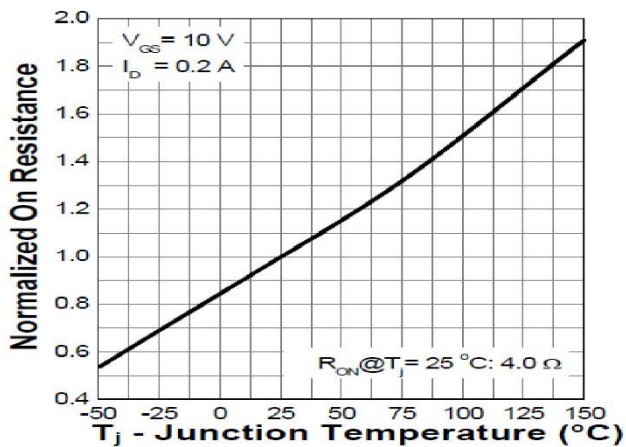


Figure 5. Drain-Source On Resistance

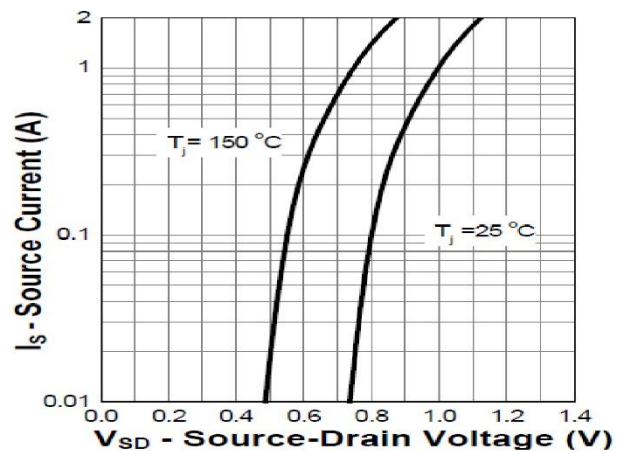


Figure 6. Source-Drain Diode Forward

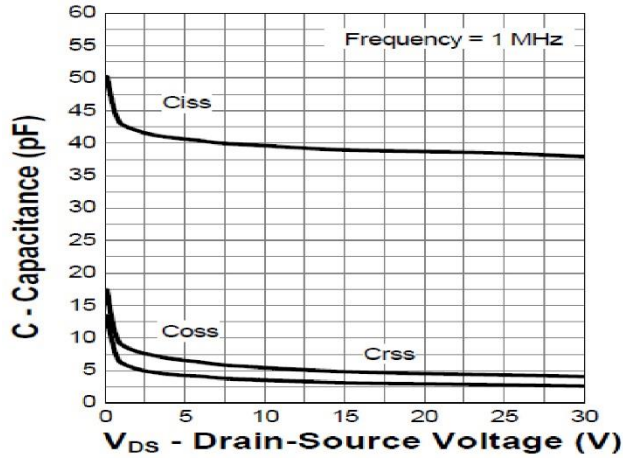


Figure 7. Capacitance

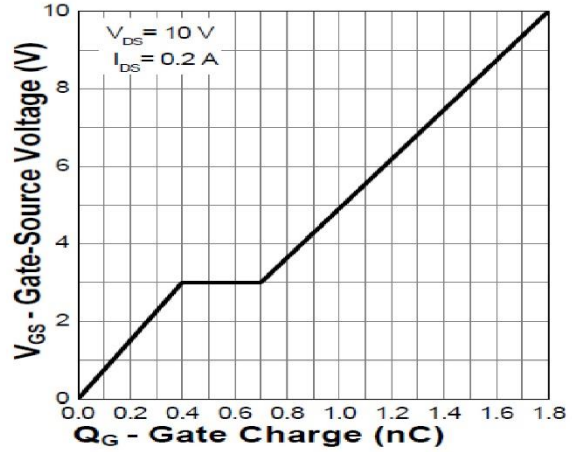


Figure 8. Gate Charge Characteristics

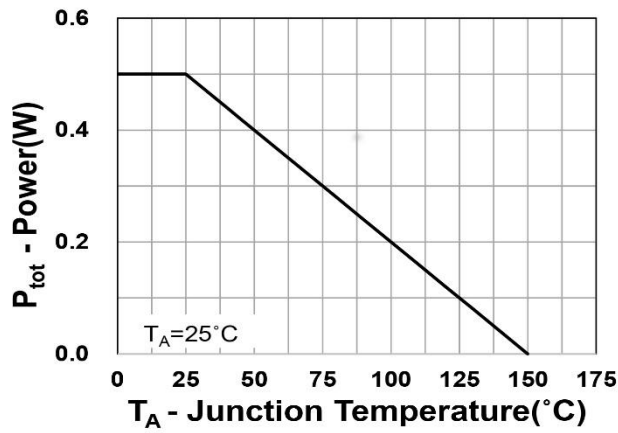


Figure 9. Power Dissipation

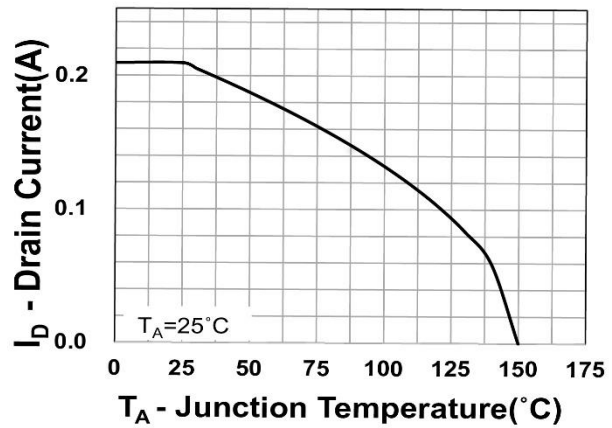


Figure 10. Drain Current

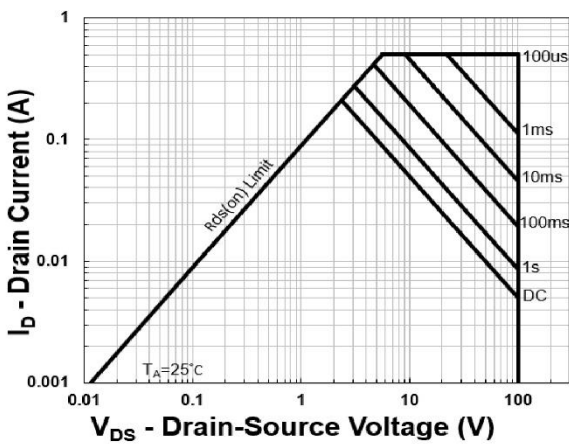


Figure 11. Safe Operating Area

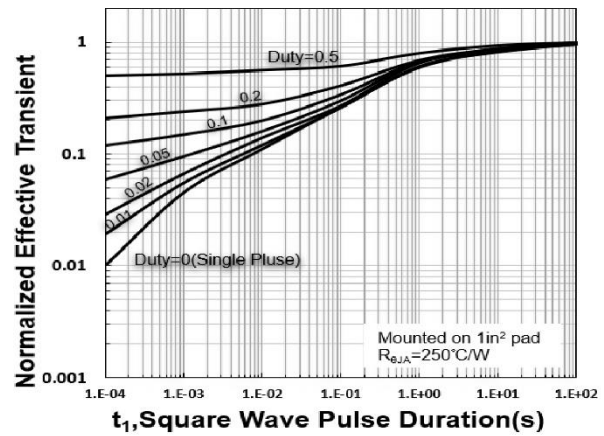


Figure 12.  $R_{\theta JA}$  Transient Thermal Impedance