



# Power MOSFETS

## DATASHEET


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LM20450PLI3A

P-Channel  
Enhancement Mode MOSFET

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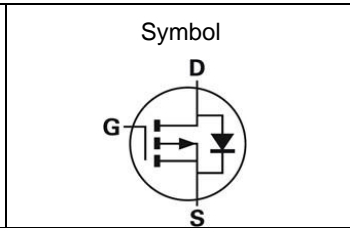
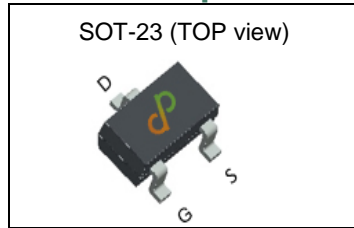


Quality Management Systems

ISO 9001:2015 Certificate

## P-Channel Enhancement Mode MOSFET

### Pin Description



### Ordering Information

Symbol	P-Channel	Unit
$V_{DSS}$	<b>-20</b>	<b>V</b>
$R_{DS(ON)-Max}$	<b>50</b>	<b>mΩ</b>
$I_D$	<b>-3.9</b>	<b>A</b>

### Feature

- Fast switching speed
- Reliable and Rugged
- ROHS Compliant & Halogen-Free

### Applications

- Portable Equipment
- Battery Powered System

### Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM20450PLI3A	SOT-23	Tape & Reel	3000 / Tape & Reel	14□□□

### Absolute Maximum Ratings (T<sub>J</sub>=25°C Unless Otherwise Noted)

Symbol	Parameter	P-Channel	Unit	
$V_{DSS}$	Drain-Source Voltage	-20	V	
$V_{GSS}$	Gate-Source Voltage	±12		
$T_J$	Maximum Junction Temperature	150	°C	
$T_{STG}$	Storage Temperature Range	-55 to 150	°C	
$I_{DM}^{①}$	Pulse Drain Current Tested	$T_A=25^{\circ}C$	-9.8	A
$I_D$	Continuous Drain Current	$T_A=25^{\circ}C$	-3.9	A
		$T_A=70^{\circ}C$	-3.1	
$P_D$	Maximum Power Dissipation	$T_A=25^{\circ}C$	1.1	W
		$T_A=70^{\circ}C$	0.7	
$I_{AS}^{②}$	Avalanche Current, Single pulse	L=0.1mH	-8	A
$E_{AS}^{②}$	Avalanche Energy, Single pulse	L=0.1mH	3.2	mJ

### Thermal Characteristics

Symbol	Parameter	Rating	Unit	
$R_{\theta JA}^{③}$	Thermal Resistance-Junction to Ambient	Steady State	110	°C/W

Note ① : Max. current is limited by junction temperature.

Note ② : UIS tested and pulse width are limited by maximum junction temperature 150°C

Note ③ : Surface Mounted on 1in<sup>2</sup> FR-4 board with 1oz.

## P-Channel Electrical Characteristics (T<sub>J</sub>=25°C Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static Electrical Characteristics</b>						
<b>BV<sub>DSS</sub></b>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>DS</sub> =-250uA	-20	-	-	V
<b>I<sub>DSS</sub></b>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-16V, V <sub>GS</sub> =0V	-	-	-1	uA
<b>V<sub>GS(th)</sub></b>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>DS</sub> =-250uA	-0.45	-0.7	-0.95	V
<b>I<sub>GSS</sub></b>	Gate Leakage Current	V <sub>GS</sub> =±12V, V <sub>DS</sub> =0V	-	-	±100	nA
<b>R<sub>DS(ON)</sub><sup>④</sup></b>	Drain-Source On-state Resistance	V <sub>GS</sub> =-4.5V, I <sub>DS</sub> =-4.2A	-	42	50	mΩ
		V <sub>GS</sub> =-2.5V, I <sub>DS</sub> =-2A	-	55	71	
		V <sub>GS</sub> =-1.8V, I <sub>DS</sub> =-1A	-	75	97	
<b>gfs</b>	Forward Transconductance	V <sub>DS</sub> =-5V, I <sub>DS</sub> =-4.2A	-	11	-	S
<b>Dynamic Characteristics<sup>⑤</sup></b>						
<b>R<sub>G</sub></b>	Gate Resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, Freq.=1MHz	-	7.6	-	Ω
<b>C<sub>iss</sub></b>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =-10V, Freq.=1MHz	-	707	-	pF
<b>C<sub>OSS</sub></b>	Output Capacitance		-	77	-	
<b>C<sub>rss</sub></b>	Reverse Transfer Capacitance		-	72	-	
<b>t<sub>d(ON)</sub></b>	Turn-on Delay Time	V <sub>GS</sub> =-4.5V, V <sub>DS</sub> =-10V, I <sub>D</sub> =-1A, R <sub>GEN</sub> =6Ω	-	5.5	-	nS
<b>t<sub>r</sub></b>	Turn-on Rise Time		-	10.2	-	
<b>t<sub>d(OFF)</sub></b>	Turn-off Delay Time		-	19.7	-	
<b>t<sub>f</sub></b>	Turn-off Fall Time		-	12.9	-	
<b>Q<sub>g</sub></b>	Total Gate Charge	V <sub>GS</sub> =-4.5V, V <sub>DS</sub> =-10V, I <sub>D</sub> =-5A	-	5.2	-	nC
<b>Q<sub>gs</sub></b>	Gate-Source Charge		-	0.6	-	
<b>Q<sub>gd</sub></b>	Gate-Drain Charge		-	1.9	-	
<b>Source-Drain Characteristics</b>						
<b>V<sub>SD</sub><sup>④</sup></b>	Diode Forward Voltage	I <sub>SD</sub> =-1A, V <sub>GS</sub> =0V	-	-0.8	-1.1	V
<b>t<sub>rr</sub></b>	Reverse Recovery Time	I <sub>F</sub> =-5A, V <sub>R</sub> =-10V	-	15.5	-	nS
<b>Q<sub>rr</sub></b>	Reverse Recovery Charge	dI <sub>F</sub> /dt=100A/μs	-	6	-	nC

Note ④ : Pulse test (pulse width≤300us, duty cycle≤2%).

Note ⑤ : Guaranteed by design, not subject to production testing.

## P-Channel Typical Characteristics

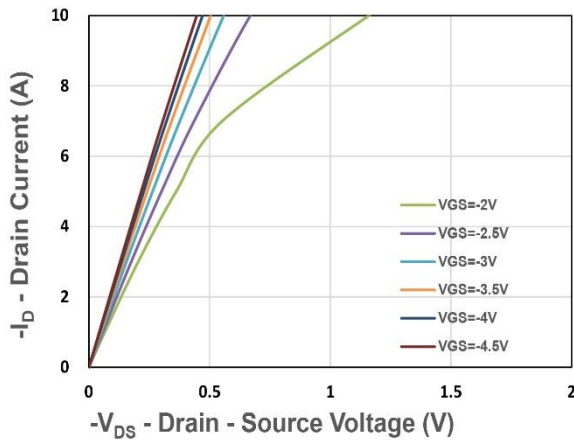


Figure 1. Output Characteristics

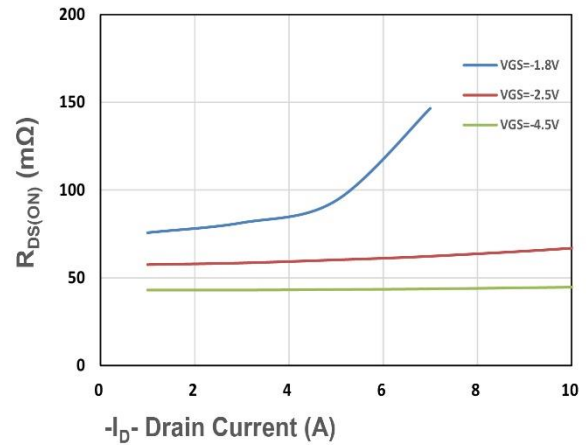


Figure 2. On-Resistance vs. ID

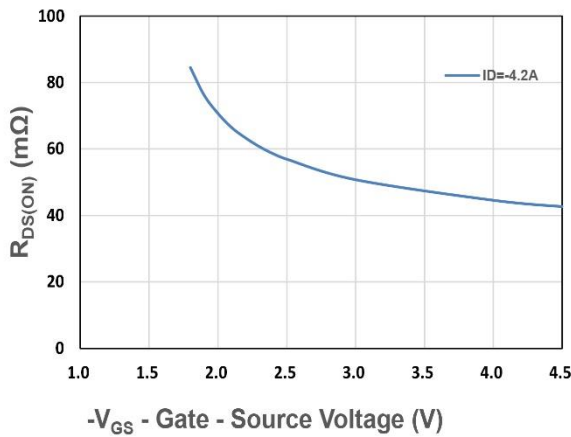


Figure 3. On-Resistance vs. VGS

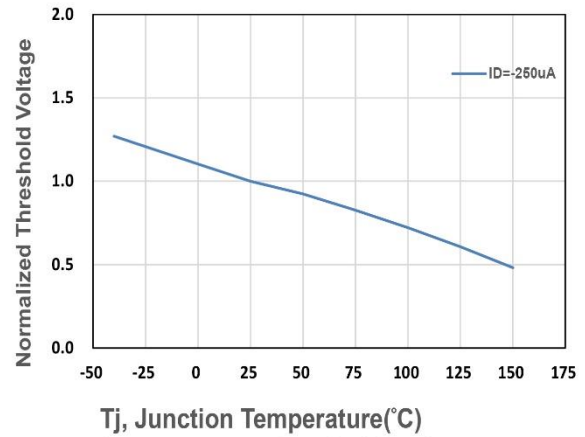


Figure 4. Gate Threshold Voltage

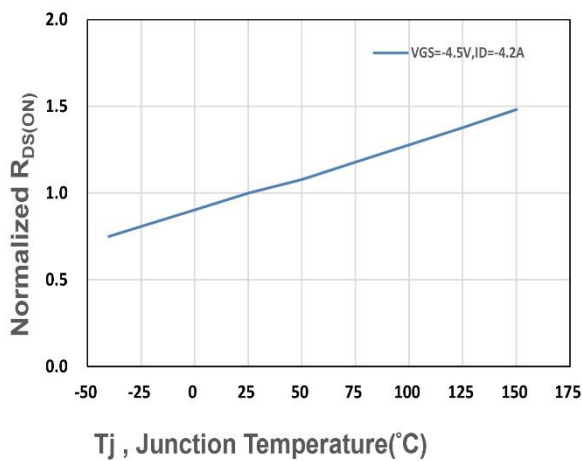


Figure 5. Drain-Source On Resistance

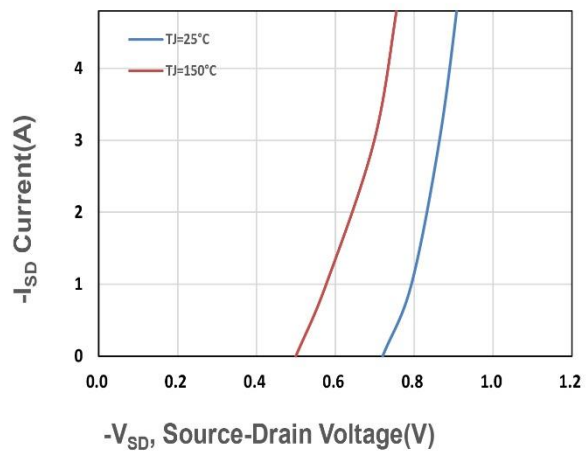
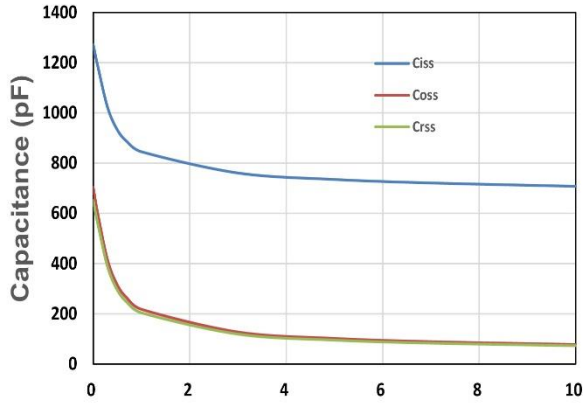
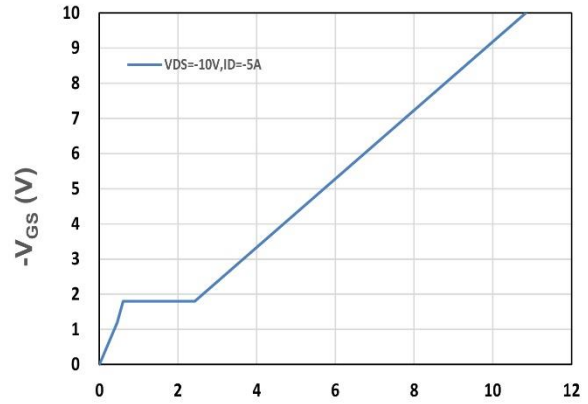


Figure 6. Source-Drain Diode Forward



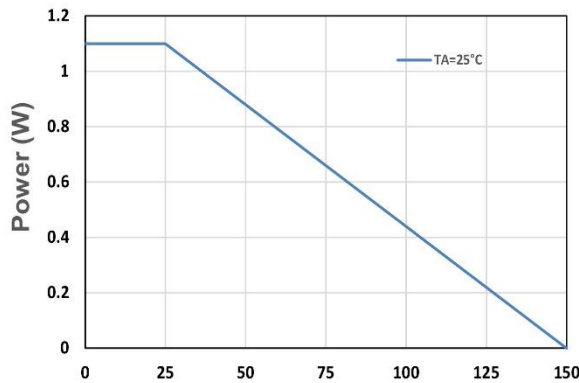
$-V_{DS}$  - Drain - Source Voltage (V)

Figure 7. Capacitance



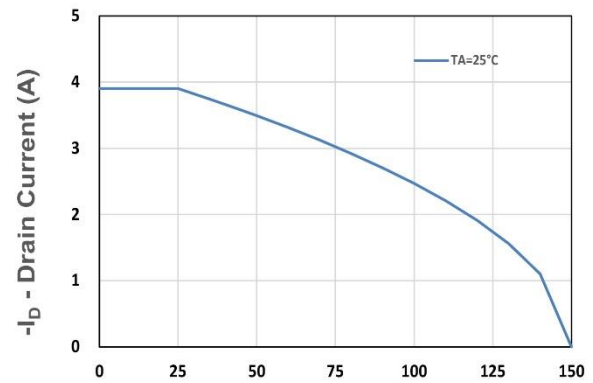
$Q_g$ , Total Gate Charge (nC)

Figure 8. Gate Charge Characteristics



$T_j$  - Junction Temperature ( $^{\circ}C$ )

Figure 9. Power Dissipation



$T_j$  - Junction Temperature ( $^{\circ}C$ )

Figure 10. Drain Current

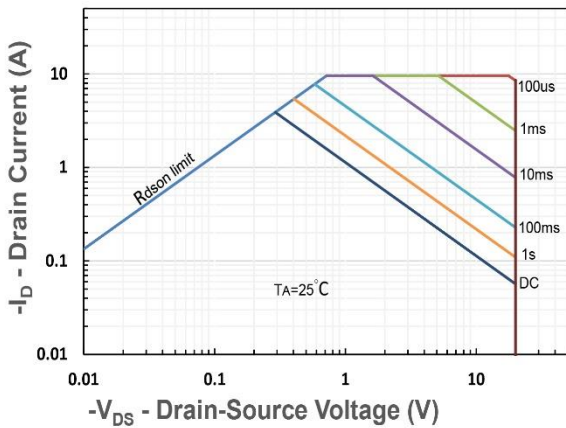


Figure 11. Safe Operating Area

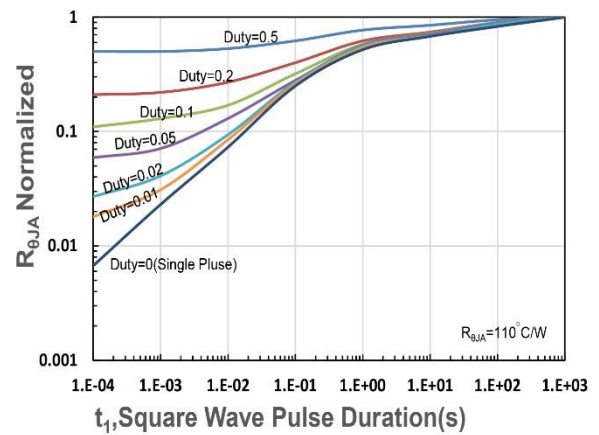


Figure 12.  $R_{\theta JA}$  Transient Thermal Impedance