# Power MOSFETS

## DATASHEET

## LM20600NLI3A

N-Channel

Enhancement Mode MOSFET

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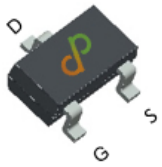
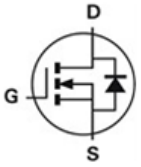
Quality Management Systems

ISO 9001:2015 Certificate

# LM20600NLI3A

## N-Channel Enhancement Mode MOSFET

### Pin Description

| SOT-23 (TOP view) | Symbol |
|---|---|
|  |  |



### Product Summary

| Symbol | N-Channel | Unit |
|---|---|---|
| $V_{DSS}$ | 20 | V |
| $R_{DS(ON)-Max}$ | 60 | mΩ |
| ID | 3.2 | A |

### Feature

- Lower Qg and Qgd for high-speed switching
- Reliable and Rugged
- ROHS Compliant & Halogen-Free

### Applications

- Portable Equipment
- Load Switch

### Ordering Information

| Orderable Part Number | Package Type | Form | Shipping | Marking |
|---|---|---|---|---|
| LM20600NLI3A | SOT-23 | Tape & Reel | 3000 / Tape & Reel | 05□□ |

### Absolute Maximum Ratings ($T_J$=25°C Unless Otherwise Noted)

| Symbol | Parameter | | N-Channel | Unit |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 20 | V |
| $V_{GSS}$ | Gate-Source Voltage | | ±12 | |
| $T_J$ | Maximum Junction Temperature | | 150 | °C |
| $T_{STG}$ | Storage Temperature Range | | -55 to 150 | °C |
| $I_{DM}$① | Pulse Drain Current Tested | $T_A$=25°C | 8 | A |
| $I_D$ | Continuous Drain Current | $T_A$=25°C | 3.2 | A |
| | | $T_A$=70°C | 2.5 | |
| $P_D$ | Maximum Power Dissipation | $T_A$=25°C | 0.9 | W |
| | | $T_A$=70°C | 0.6 | |
| $I_{AS}$② | Avalanche Current, Single pulse | L=0.1mH | 12 | A |
| $E_{AS}$② | Avalanche Energy, Single pulse | L=0.1mH | 7.2 | mJ |

### Thermal Characteristics

| Symbol | Parameter | | Rating | Unit |
|---|---|---|---|---|
| $R_{\theta JA}$③ | Thermal Resistance-Junction to Ambient | t≦10sec | 100 | °C/W |
| | | Steady State | 140 | °C/W |

Note ①：Max. current is limited by junction temperature

Note ②：UIS tested and pulse width are limited by maximum junction temperature 150°C

Note ③：Surface Mounted on 1in$^2$ FR-4 board with 1oz.

## N-Channel Electrical Characteristics ($T_J$=25°C Unless Otherwise Noted)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Static Electrical Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$=0V, $I_{DS}$=250uA | 20 | - | - | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$=16V, $V_{GS}$=0V | - | - | 1 | uA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$, $I_{DS}$=250uA | 0.5 | 0.7 | 1 | V |
| $I_{GSS}$ | Gate Leakage Current | $V_{GS}$=±12V, $V_{DS}$=0V | - | - | ±100 | nA |
| $R_{DS(ON)}$④ | Drain-Source On-state Resistance | $V_{GS}$=4.5V, $I_{DS}$=3A | - | 50 | 60 | mΩ |
| | | $V_{GS}$=2.5V, $I_{DS}$=2A | - | 66 | 86 | |
| gfs | Forward Transconductance | $V_{DS}$=5V, $I_{DS}$=3A | - | 7 | - | S |
| **Dynamic Characteristics** ⑤ | | | | | | |
| $R_G$ | Gate Resistance | $V_{GS}$=0V,$V_{DS}$=0V, Freq.=1MHz | - | 1.3 | - | Ω |
| $C_{iss}$ | Input Capacitance | $V_{GS}$=0V, $V_{DS}$=10V, Freq.=1MHz | - | 123 | - | pF |
| $C_{oss}$ | Output Capacitance | | - | 30 | - | |
| $C_{rss}$ | Reverse Transfer Capacitance | | - | 26 | - | |
| $td_{(ON)}$ | Turn-on Delay Time | $V_{GS}$=10V,$V_{DS}$=10V, $I_D$=1A,$R_{GEN}$=6Ω | - | 3.2 | - | nS |
| $t_r$ | Turn-on Rise Time | | - | 2.6 | - | |
| $t_{d(OFF)}$ | Turn-off Delay Time | | - | 10 | - | |
| $t_f$ | Turn-off Fall Time | | - | 5 | - | |
| $Q_g$ | Total Gate Charge | $V_{GS}$=2.5V,$V_{DS}$=10V $I_D$=3A | - | 1.8 | - | nC |
| $Q_g$ | Total Gate Charge | $V_{GS}$=4.5V,$V_{DS}$=10V, $I_D$=3A | - | 3.0 | - | |
| Qgs | Gate-Source Charge | | - | 0.5 | - | |
| Qgd | Gate-Drain Charge | | - | 0.9 | - | |
| **Source-Drain Characteristics** | | | | | | |
| $V_{SD}$④ | Diode Forward Voltage | $I_{SD}$=3A, $V_{GS}$=0V | - | 0.8 | 1.1 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_F$=3A, $V_R$=0V dI$_F$/dt=100A/μs | - | 11.6 | - | nS |
| $Q_{rr}$ | Reverse Recovery Charge | | - | 3.6 | - | nC |

Note ④：Pulse test (pulse width≤300us, duty cycle≤2%).
Note ⑤：Guaranteed by design, not subject to production testing.

## N-Channel Typical Characteristics

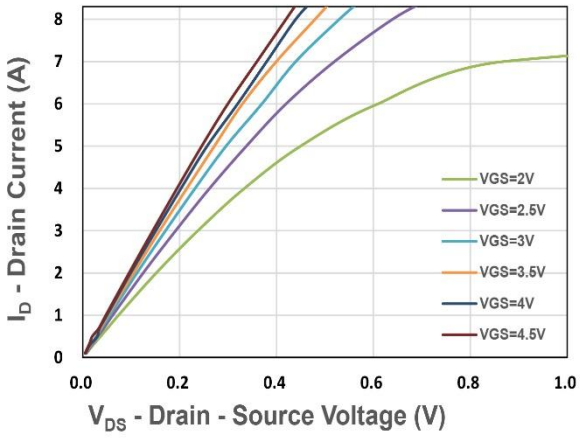



Figure 1. Output Characteristics

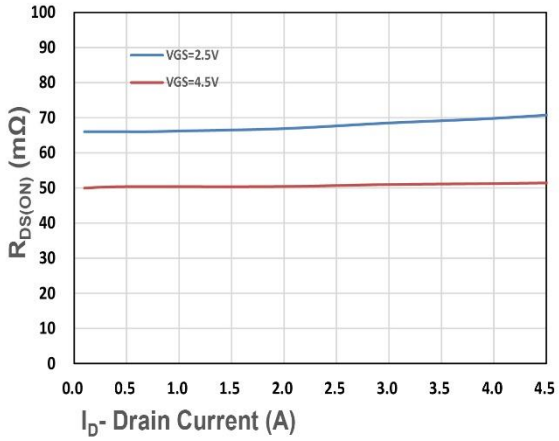



Figure 2. On-Resistance vs. ID

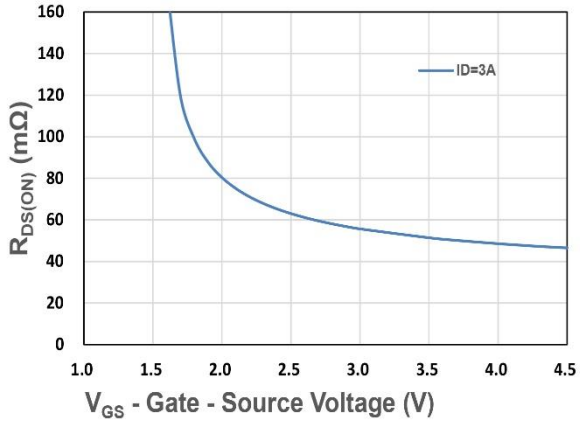



Figure 3. On-Resistance vs. VGS

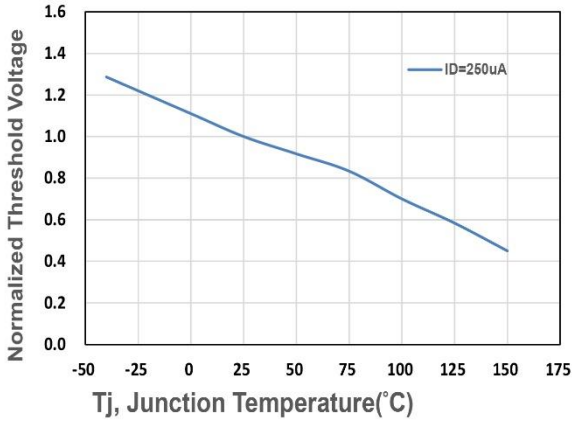



Figure 4. Gate Threshold Voltage

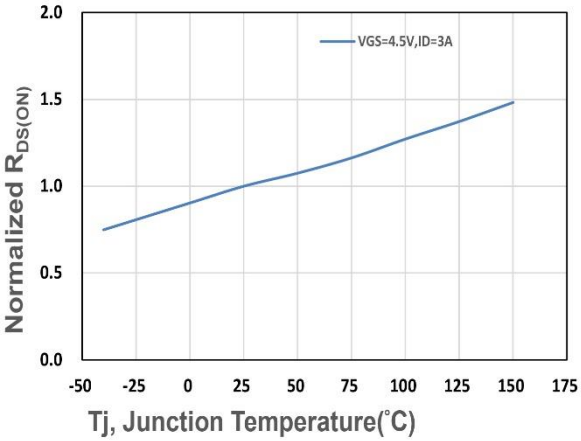



Figure 5. Drain-Source On Resistance

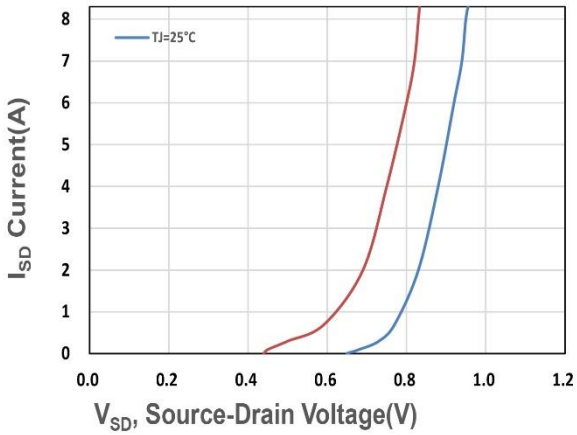



Figure 6. Source-Drain Diode Forward

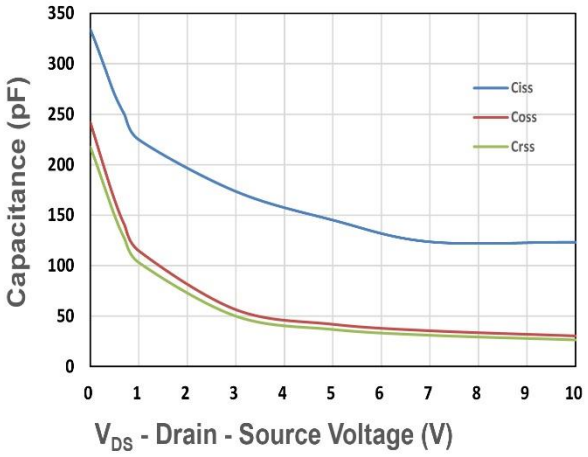



Figure 7. Capacitance

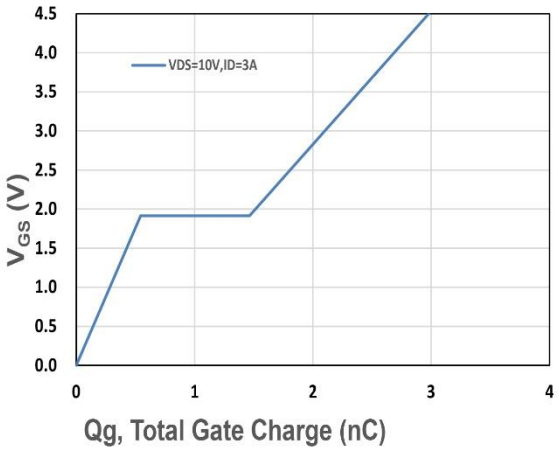



Figure 8. Gate Charge Characteristics

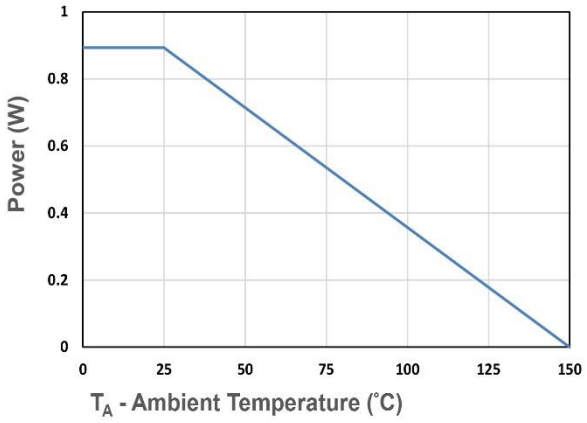



Figure 9. Power Dissipation

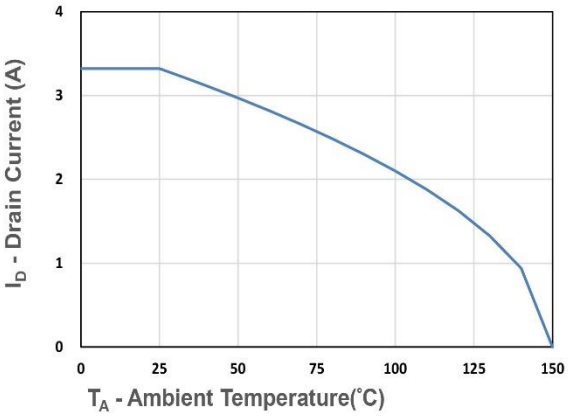



Figure 10. Drain Current

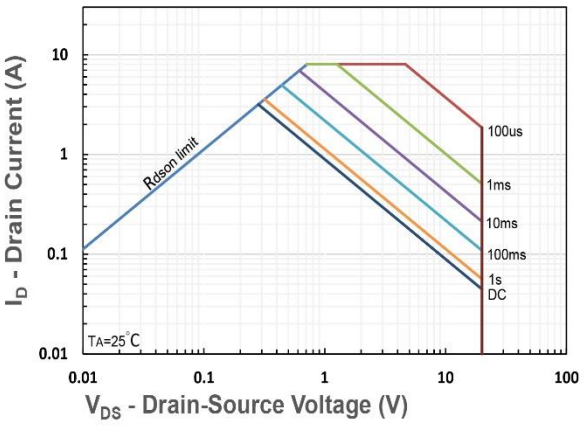



Figure 11. Safe Operating Area

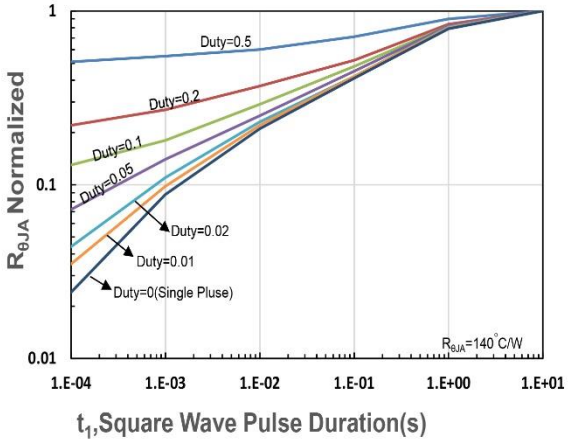



Figure 12. RθJA Transient Thermal Impedance