



Power MOSFETS

DATASHEET

LM20F40PGA3A

N-Channel
Enhancement Mode MOSFET

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Quality Management Systems
ISO 9001:2015 Certificate

P-Channel Enhancement Mode MOSFET

Pin Description

FBP1006 (TOP view)	Symbol	Product Summary												
		<table border="1"> <thead> <tr> <th>Symbol</th> <th>P-Channel</th> <th>Unit</th> </tr> </thead> <tbody> <tr> <td>V_{DSS}</td> <td>-20</td> <td>V</td> </tr> <tr> <td>$R_{DS(ON)-Max}$</td> <td>640</td> <td>$\text{m}\Omega$</td> </tr> <tr> <td>ID</td> <td>-0.85</td> <td>A</td> </tr> </tbody> </table>	Symbol	P-Channel	Unit	V_{DSS}	-20	V	$R_{DS(ON)-Max}$	640	$\text{m}\Omega$	ID	-0.85	A
Symbol	P-Channel	Unit												
V_{DSS}	-20	V												
$R_{DS(ON)-Max}$	640	$\text{m}\Omega$												
ID	-0.85	A												

Feature

- Surface mount package
- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- ESD Protection

Applications

- Small Signal Switch
- Load Switch

Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM20F40PGA3A	FBP1006	Tape & Reel	10000 / Tape & Reel	<input type="checkbox"/> 4

Absolute Maximum Ratings ($T_J=25^\circ\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	P-Channel	Unit
V_{DSS}	Drain-Source Voltage	-20	V
V_{GSS}	Gate-Source Voltage	± 12	
T_J	Maximum Junction Temperature	150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$I_{DM}^{(1)}$	Pulse Drain Current Tested	$T_A=25^\circ\text{C}$	A
I_D	Continuous Drain Current	$T_A=25^\circ\text{C}$	-0.85
		$T_A=70^\circ\text{C}$	-0.68
P_D	Maximum Power Dissipation	$T_A=25^\circ\text{C}$	0.69
		$T_A=70^\circ\text{C}$	0.44

Thermal Characteristics

Symbol	Parameter	Rating	Unit
$R_{\theta JA}^{(2)}$	Thermal Resistance-Junction to Ambient	Steady State	$^\circ\text{C}/\text{W}$

Note ① : Max. current is limited by junction temperature.

Note ② : Surface Mounted on 1in² FR-4 board with 1oz.

P-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Electrical Characteristics						
$\mathbf{BV_{DSS}}$	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$, $I_{DS}=-250\mu\text{A}$	-20	-	-	V
$\mathbf{I_{DSS}}$	Zero Gate Voltage Drain Current	$V_{DS}=-16\text{V}$, $V_{GS}=0\text{V}$	-	-	-1	μA
$\mathbf{V_{GS(th)}}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_{DS}=-250\mu\text{A}$	-0.5	-0.75	-1	V
$\mathbf{I_{GSS}}$	Gate Leakage Current	$V_{GS}=\pm 12\text{V}$, $V_{DS}=0\text{V}$	-	-	± 10	μA
$\mathbf{R_{DS(ON)}}^{\circledast}$	Drain-Source On-state Resistance	$V_{GS}=-4.5\text{V}$, $I_{DS}=-550\text{mA}$	-	530	640	$\text{m}\Omega$
		$V_{GS}=-2.5\text{V}$, $I_{DS}=-450\text{mA}$	-	730	950	
		$V_{GS}=-1.8\text{V}$, $I_{DS}=-350\text{mA}$	-	1300	1950	
$\mathbf{g_{fs}}$	Forward Transconductance	$V_{DS}=-5\text{V}$, $I_{DS}=-550\text{mA}$	-	1	-	S
Dynamic Characteristics ^④						
$\mathbf{C_{iss}}$	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=-10\text{V}$, Freq.=1MHz	-	58	-	pF
$\mathbf{C_{oss}}$	Output Capacitance		-	5.7	-	
$\mathbf{C_{rss}}$	Reverse Transfer Capacitance		-	4.4	-	
$\mathbf{t_{d(ON)}}$	Turn-on Delay Time	$V_{GS}=-4.5\text{V}$, $V_{DS}=-10\text{V}$, $I_D=-1\text{A}$, $R_{GEN}=6\Omega$	-	0.4	-	uS
$\mathbf{t_r}$	Turn-on Rise Time		-	0.06	-	
$\mathbf{t_{d(OFF)}}$	Turn-off Delay Time		-	0.02	-	
$\mathbf{t_f}$	Turn-off Fall Time		-	0.8	-	
$\mathbf{Q_g}$	Total Gate Charge	$V_{GS}=-2.5\text{V}$, $V_{DS}=-10\text{V}$ $I_D=-1\text{A}$	-	0.53	-	nC
$\mathbf{Q_g}$	Total Gate Charge	$V_{GS}=-4.5\text{V}$, $V_{DS}=-10\text{V}$, $I_D=-1\text{A}$	-	0.8	-	
$\mathbf{Q_{gs}}$	Gate-Source Charge		-	0.2	-	
$\mathbf{Q_{gd}}$	Gate-Drain Charge		-	0.2	-	
Source-Drain Characteristics						
$\mathbf{V_{SD}}^{\circledast}$	Diode Forward Voltage	$I_{SD}=-1\text{A}$, $V_{GS}=0\text{V}$	-	-0.75	-1.1	V
$\mathbf{t_{rr}}$	Reverse Recovery Time	$I_F=-1\text{A}$, $V_R=0\text{V}$ $dI_F/dt=100\text{A}/\mu\text{s}$	-	9.2	-	nS
$\mathbf{Q_{rr}}$	Reverse Recovery Charge		-	0.8	-	nC

Note ④ : Pulse test (pulse width $\leq 300\text{us}$, duty cycle $\leq 2\%$).

Note ⑤ : Guaranteed by design, not subject to production testing.

P-Channel Typical Characteristics

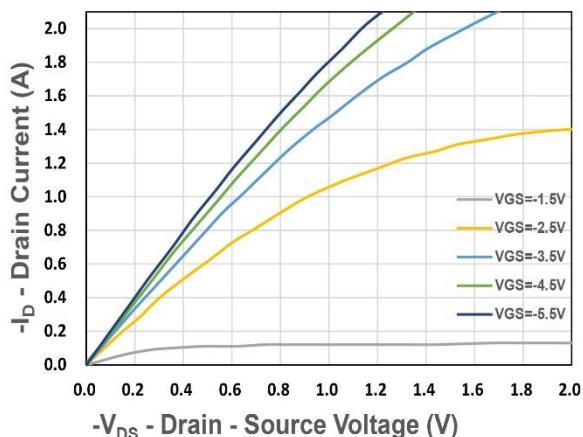


Figure 1. Output Characteristics

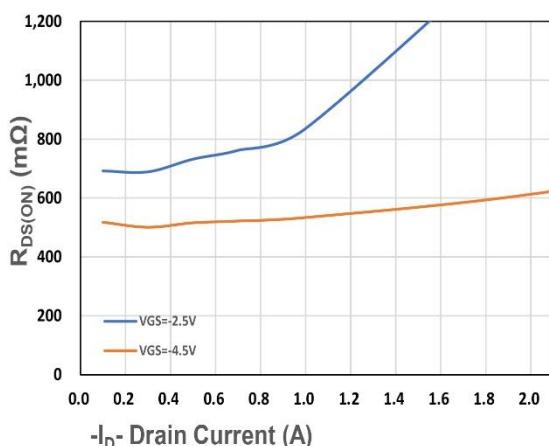


Figure 2. On-Resistance vs. ID

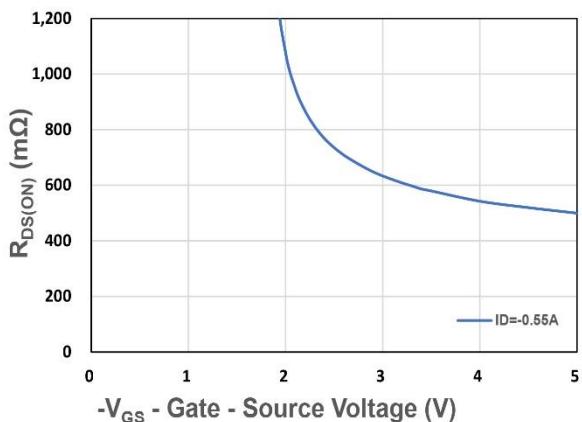


Figure 3. On-Resistance vs. VGS

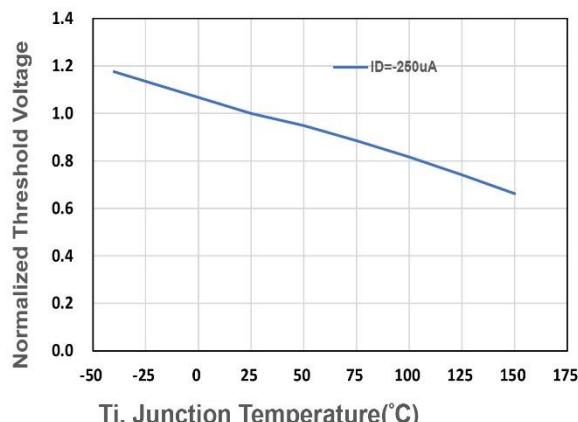


Figure 4. Gate Threshold Voltage

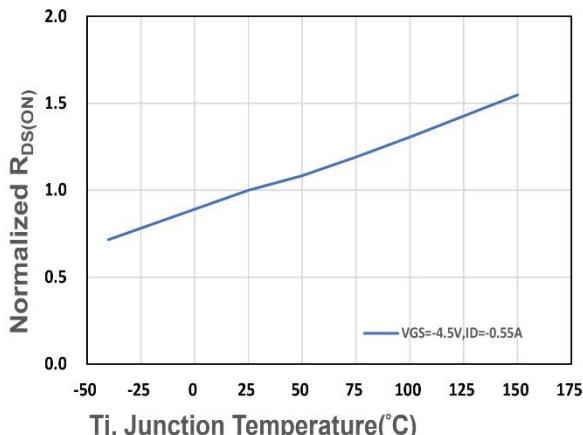


Figure 5. Drain-Source On Resistance

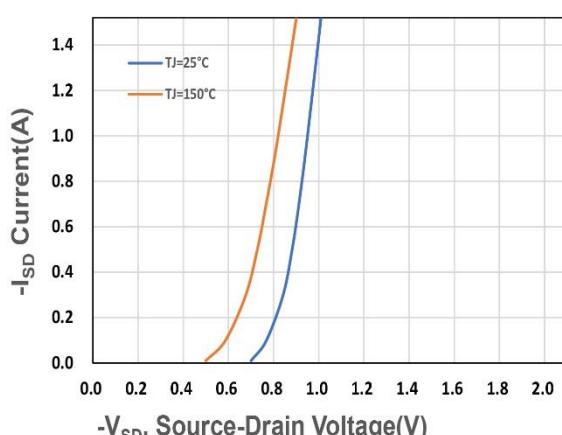


Figure 6. Source-Drain Diode Forward

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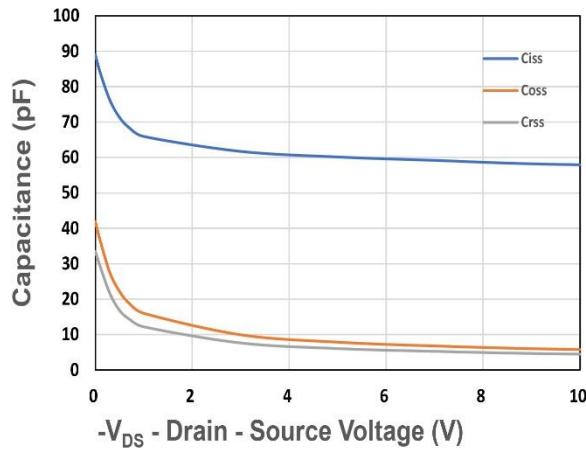


Figure 7. Capacitance

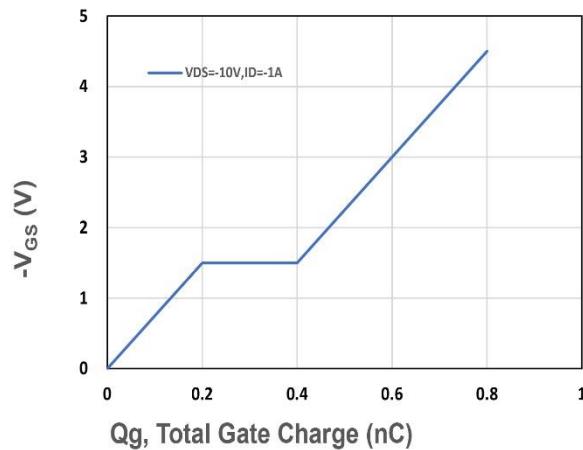


Figure 8. Gate Charge Characteristics

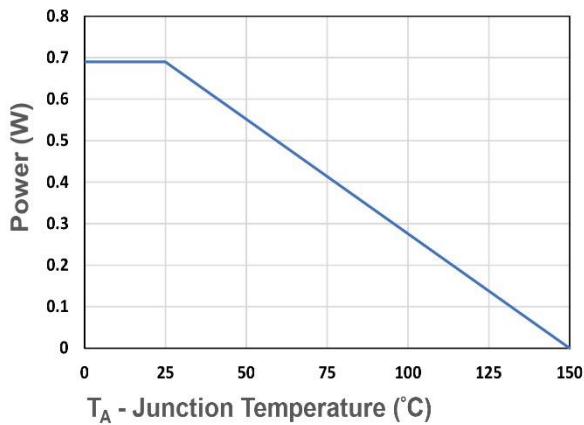


Figure 9. Power Dissipation

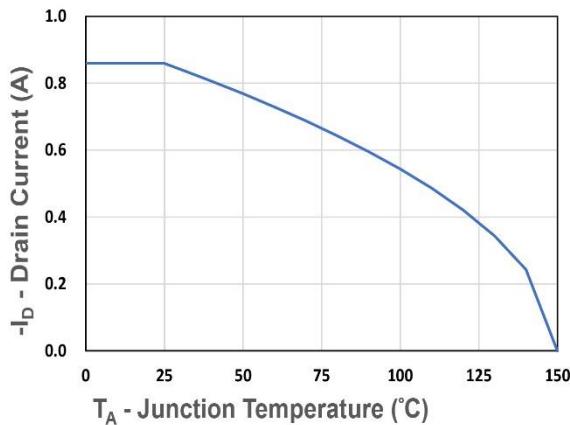


Figure 10. Drain Current

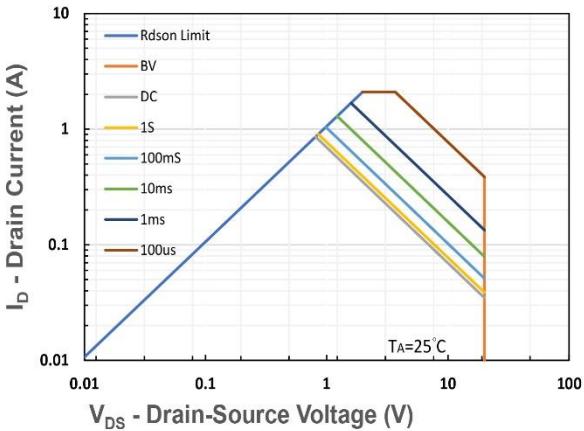


Figure 11. Safe Operating Area

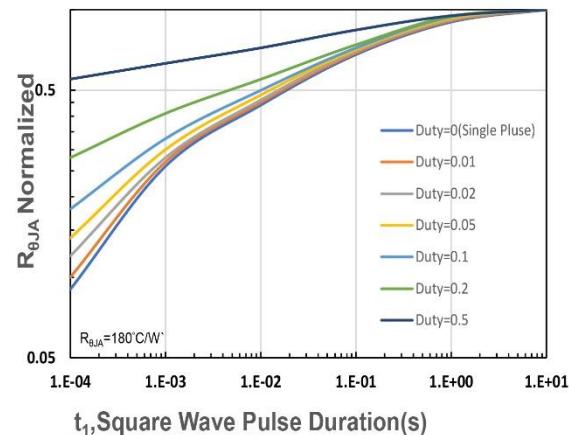


Figure 12. $R_{\theta JA}$ Transient Thermal Impedance