




# Power MOSFETS


## DATASHEET


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**LM30145PAK8A**

P-Channel  
Enhancement Mode MOSFET

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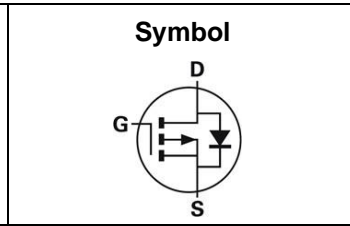
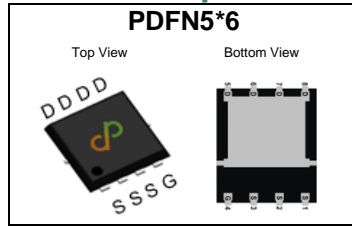


Quality Management Systems

ISO 9001:2015 Certificate

## P-Channel Enhancement Mode MOSFET

### Pin Description



### Ordering Information

Symbol	N-Channel	Unit
$V_{DSS}$	-30	V
$R_{DS(ON)-Max}$	14.5	m $\Omega$
$I_D$	-43	A

### Feature

- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- Lower  $Q_g$  and  $Q_{gd}$  for high-speed switching
- Lower  $R_{DS(ON)}$  to Minimize Conduction Losses
- 100% UIS Tested

### Applications

- Power Management in DC/DC
- Power Load Switch

### Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM30145PAK8A	PDFN5*6	Tape & Reel	5000 / Tape & Reel	30145 □□□□□□

### Absolute Maximum Ratings (T<sub>J</sub>=25°C Unless Otherwise Noted)

Symbol	Parameter	P-Channel	Unit
$V_{DSS}$	Drain-Source Voltage	-30	V
$V_{GSS}$	Gate-Source Voltage	±25	
$T_J$	Maximum Junction Temperature	150	°C
$T_{STG}$	Storage Temperature Range	-55 to 150	°C
$I_{DM}^{①}$	Pulse Drain Current Tested	$T_c=25^\circ\text{C}$ -70	A
$I_D^{②}$	Continuous Drain Current	$T_c=25^\circ\text{C}$ -43	A
		$T_c=100^\circ\text{C}$ -27	
$P_D^{③}$	Maximum Power Dissipation	$T_c=25^\circ\text{C}$ 42	W
		$T_c=100^\circ\text{C}$ 17	
$I_{AS}^{③}$	Avalanche Current, Single pulse	L=0.1mH -26	A
$E_{AS}^{②}$	Avalanche Energy, Single pulse	L=0.1mH 34	mJ

### Thermal Characteristics

Symbol	Parameter	Rating	Unit
$R_{\theta JC}$	Thermal Resistance-Junction to Case	Steady State 3	°C/W
$R_{\theta JA}^{③}$	Thermal Resistance-Junction to Ambient	Steady State 50	°C/W

Note ① : Max. current is limited by bonding wire

Note ② : UIS tested and pulse width are limited by maximum junction temperature 150°C

Note ③ : Surface Mounted on 1in<sup>2</sup> FR-4 board with 1oz.

## P-Channel Electrical Characteristics (T<sub>J</sub>=25°C Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static Electrical Characteristics</b>						
<b>BV<sub>DSS</sub></b>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>DS</sub> =-250uA	-30	-	-	V
<b>I<sub>DSS</sub></b>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-24V, V <sub>GS</sub> =0V	-	-	-1	uA
<b>V<sub>GS(th)</sub></b>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>DS</sub> =-250uA	-1	-1.5	-2	V
<b>I<sub>GSS</sub></b>	Gate Leakage Current	V <sub>GS</sub> =±25V, V <sub>DS</sub> =0V	-	-	±100	nA
<b>R<sub>DS(ON)</sub><sup>④</sup></b>	Drain-Source On-state Resistance	V <sub>GS</sub> =-10V, I <sub>DS</sub> =-10A	-	12	14.5	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>DS</sub> =-7A	-	15.5	20	
<b>g<sub>fs</sub></b>	Forward Transconductance	V <sub>DS</sub> =-10V, I <sub>DS</sub> =-5A	-	14.7	-	S
<b>Dynamic Characteristics<sup>®</sup></b>						
<b>R<sub>G</sub></b>	Gate Resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, Freq.=1MHz	-	8.9	-	Ω
<b>C<sub>iss</sub></b>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =-15V, Freq.=1MHz	-	2157	-	pF
<b>C<sub>oss</sub></b>	Output Capacitance					
<b>C<sub>rss</sub></b>	Reverse Transfer Capacitance					
<b>t<sub>d(ON)</sub></b>	Turn-on Delay Time	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-15V, I <sub>D</sub> =-20A, R <sub>GEN</sub> =3.3Ω	-	10.6	-	nS
<b>t<sub>r</sub></b>	Turn-on Rise Time					
<b>t<sub>d(OFF)</sub></b>	Turn-off Delay Time					
<b>t<sub>f</sub></b>	Turn-off Fall Time					
<b>Q<sub>g</sub></b>	Total Gate Charge	V <sub>GS</sub> =-4.5V, V <sub>DS</sub> =-15V, I <sub>D</sub> =-20A	-	23	-	nC
<b>Q<sub>g</sub></b>	Total Gate Charge	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-15V, I <sub>D</sub> =-20A	-	46	-	
<b>Q<sub>gs</sub></b>	Gate-Source Charge		-	6.5	-	
<b>Q<sub>gd</sub></b>	Gate-Drain Charge		-	8.8	-	
<b>Source-Drain Characteristics</b>						
<b>V<sub>SD</sub><sup>④</sup></b>	Diode Forward Voltage	I <sub>SD</sub> =-3A, V <sub>GS</sub> =0V	-	-0.75	-1.1	V
<b>t<sub>rr</sub></b>	Reverse Recovery Time	I <sub>F</sub> =-10A, V <sub>R</sub> =-15V,	-	13.4	-	nS
<b>Q<sub>rr</sub></b>	Reverse Recovery Charge	dI <sub>F</sub> /dt=1A/μs	-	7.1	-	nC

Note ④ : Pulse test (pulse width≤300us, duty cycle≤2%).

Note ⑤ : Guaranteed by design, not subject to production testing.

## P-Channel Typical Characteristics

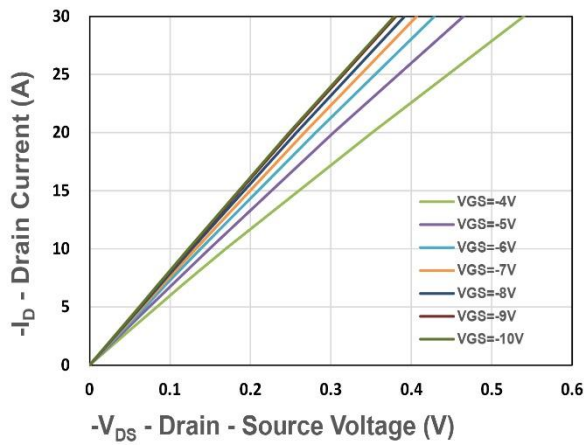


Figure 1. Output Characteristics

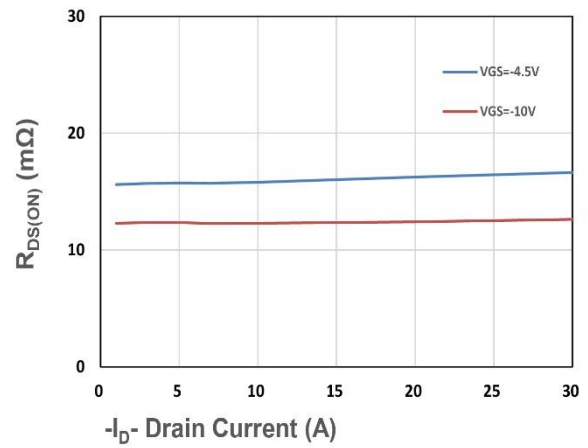


Figure 2. On-Resistance vs. ID

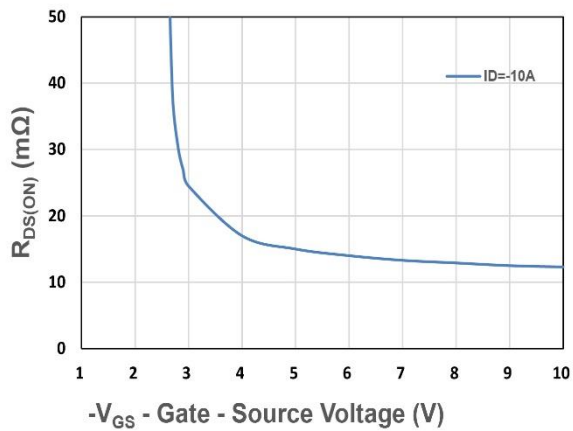


Figure 3. On-Resistance vs. VGS

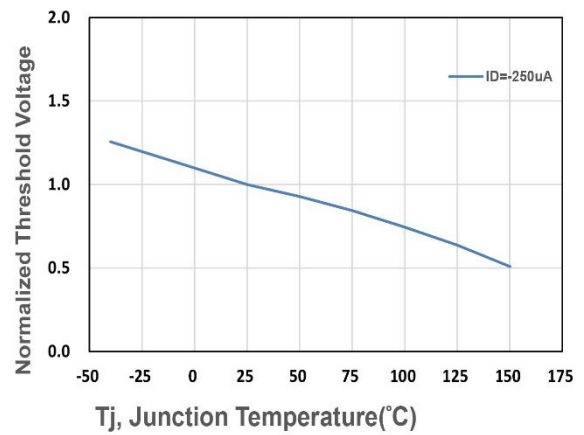


Figure 4. Gate Threshold Voltage

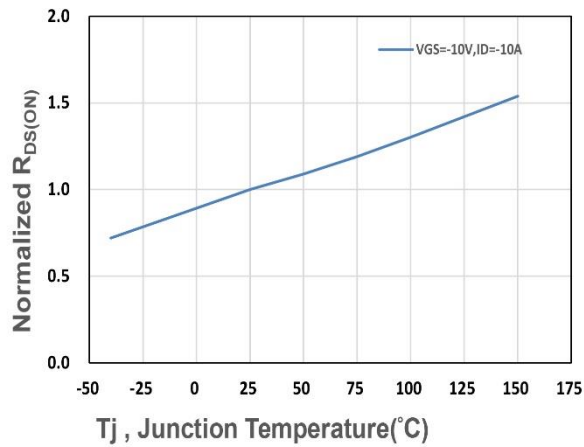


Figure 5. Drain-Source On Resistance

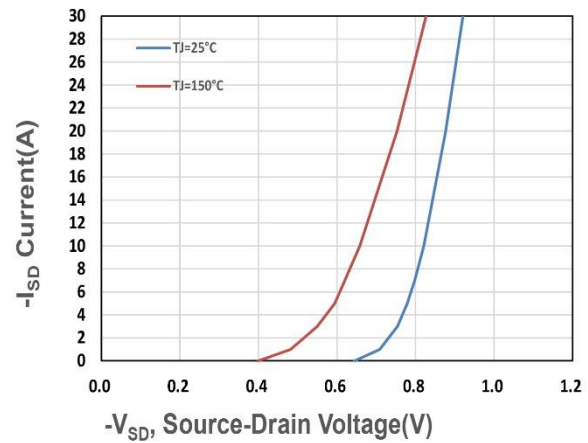
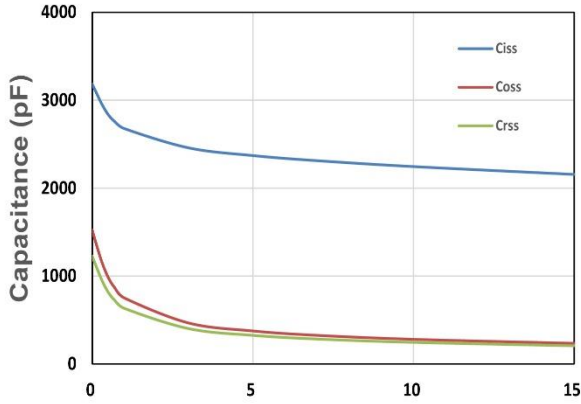
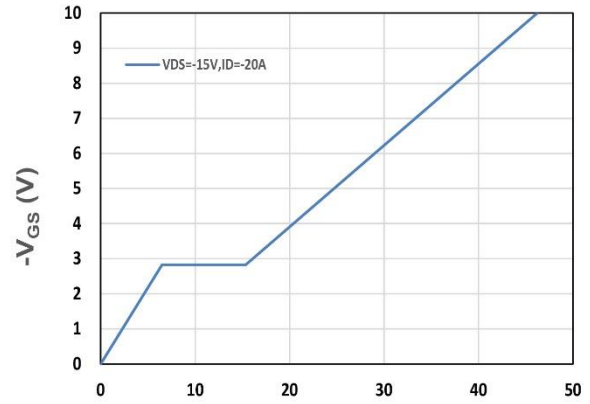


Figure 6. Source-Drain Diode Forward



-V<sub>DS</sub> - Drain - Source Voltage (V)

Figure 7. Capacitance



Qg, Total Gate Charge (nC)

Figure 8. Gate Charge Characteristics

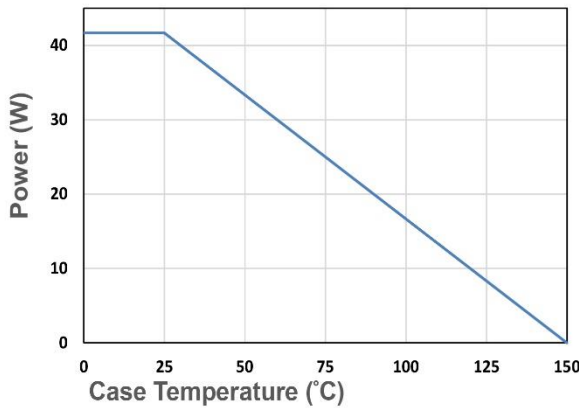


Figure 9. Power Dissipation

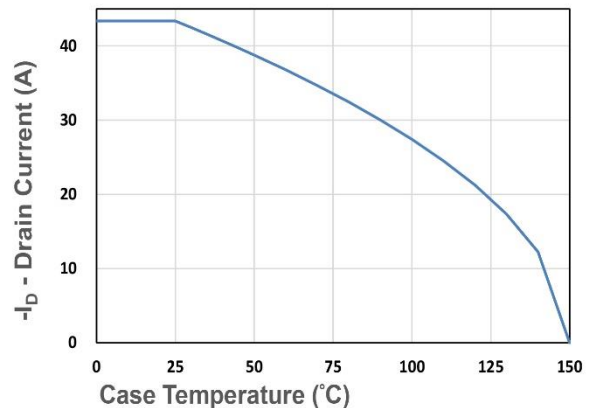
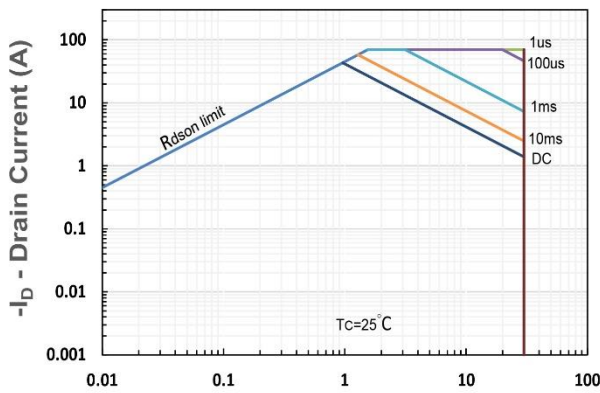
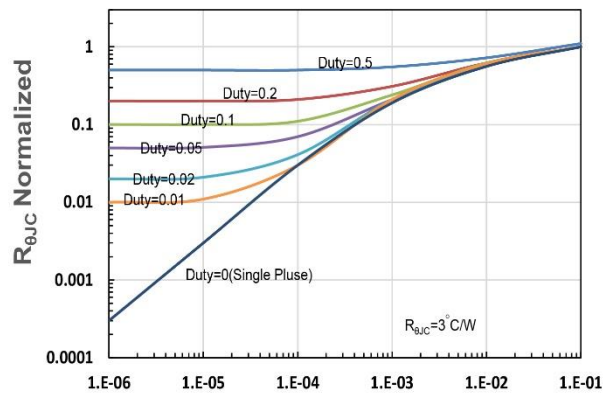


Figure 10. Drain Current



-V<sub>DS</sub> - Drain-Source Voltage (V)

Figure 11. Safe Operating Area



t<sub>1</sub>, Square Wave Pulse Duration (s)

Figure 12. R<sub>θJC</sub> Transient Thermal Impedance