




Power MOSFETS


DATASHEET

LM40160PAO2A

P-Channel
Enhancement Mode MOSFET

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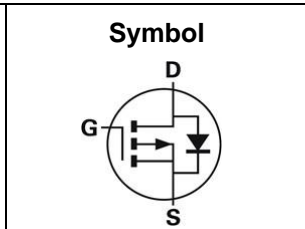
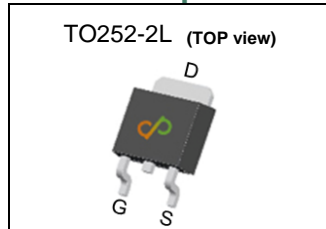


Quality Management Systems

ISO 9001:2015 Certificate

P-Channel Enhancement Mode MOSFET

Pin Description



Product Summary

Symbol	P-Channel	Unit
V_{DSS}	-40	V
$R_{DS(ON)-Max}$	16	m Ω
I_D	-38	A

Feature

- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- 100% UIS and Tested

Applications

- Load Switches
- BLDC Motor

Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM40160PAO2A	TO252-2L	Tape & Reel	3000 / Tape & Reel	40160 □□□□□□

Absolute Maximum Ratings ($T_J=25^\circ\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	P-Channel	Unit
V_{DSS}	Drain-Source Voltage	-40	V
V_{GSS}	Gate-Source Voltage	± 20	
T_J	Maximum Junction Temperature	150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$I_{DM}^{①}$	Pulse Drain Current Tested	$T_c=25^\circ\text{C}$	A
I_D	Continuous Drain Current	$T_c=25^\circ\text{C}$	A
		$T_c=100^\circ\text{C}$	-24
P_D	Maximum Power Dissipation	$T_c=25^\circ\text{C}$	W
		$T_c=100^\circ\text{C}$	15
$I_{AS}^{②}$	Avalanche Current, Single pulse	$L=0.1\text{mH}$	A
$E_{AS}^{②}$	Avalanche Energy, Single pulse	$L=0.1\text{mH}$	mJ

Thermal Characteristics

Symbol	Parameter	Rating	Unit
$R_{\theta JC}$	Thermal Resistance-Junction to Case	Steady State	$^\circ\text{C/W}$
$R_{\theta JA}^{③}$	Thermal Resistance-Junction to Ambient	Steady State	$^\circ\text{C/W}$

Note ① : Max. current is limited by junction temperature.

Note ② : UIS tested and pulse width are limited by maximum junction temperature 150°C

Note ③ : Surface Mounted on 1in^2 FR-4 board with 1oz.

P-Channel Electrical Characteristics (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Electrical Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =-250uA	-40	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-32V, V _{GS} =0V	-	-	-1	uA
V_{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =-250uA	-1	-1.7	-2.3	V
I_{GSS}	Gate Leakage Current	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
R_{DS(ON)}^④	Drain-Source On-state Resistance	V _{GS} =-10V, I _{DS} =-25A	-	13.5	16	mΩ
		V _{GS} =-4.5V, I _{DS} =-15A	-	16	20	
g_{fs}	Forward Transconductance	V _{DS} =-5V, I _{DS} =-12.5A	-	2.43	-	S
Dynamic Characteristics[®]						
R_G	Gate Resistance	V _{GS} =0V, V _{DS} =0V, Freq.=1MHz	-	5.5	-	Ω
C_{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-20V, Freq.=1MHz	-	2440	-	pF
C_{oss}	Output Capacitance					
C_{rss}	Reverse Transfer Capacitance					
t_{d(ON)}	Turn-on Delay Time	V _{GS} =-10V, V _{DS} =-20V, I _D =-1A, R _{GEN} =6Ω	-	6.5	-	nS
t_r	Turn-on Rise Time					
t_{d(OFF)}	Turn-off Delay Time					
t_f	Turn-off Fall Time					
Q_g	Total Gate Charge	V _{GS} =-4.5V, V _{DS} =-20V, I _D =-25A	-	25.4	-	nC
Q_g	Total Gate Charge	V _{GS} =-10V, V _{DS} =-20V, I _D =-25A	-	53.2	-	
Q_{gs}	Gate-Source Charge		-	10.85	-	
Q_{gd}	Gate-Drain Charge		-	8.63	-	
Source-Drain Characteristics						
V_{SD}^④	Diode Forward Voltage	I _{SD} =-12.5A, V _{GS} =0V	-	-0.8	-1.1	V
t_{rr}	Reverse Recovery Time	I _F =-12.5A, V _R =-20V	-	18.1	-	nS
Q_{rr}	Reverse Recovery Charge	dI _F /dt=100A/μs	-	8.9	-	nC

Note ④ : Pulse test (pulse width≤300us, duty cycle≤2%).

Note ⑤ : Guaranteed by design, not subject to production testing.

P-Channel Typical Characteristics

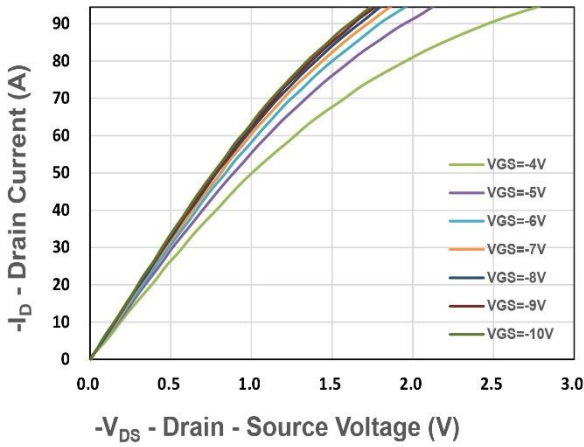


Figure 1. Output Characteristics

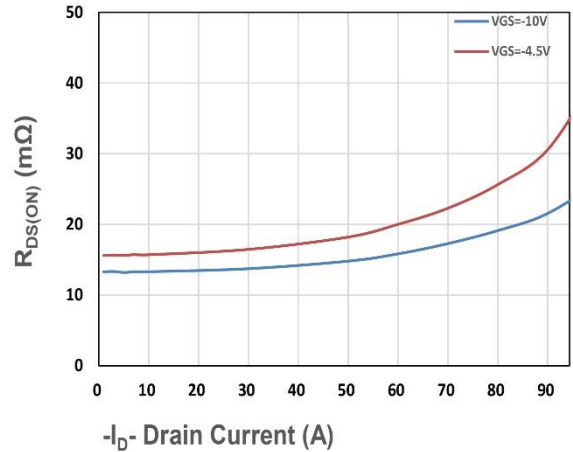


Figure 2. On-Resistance vs. ID

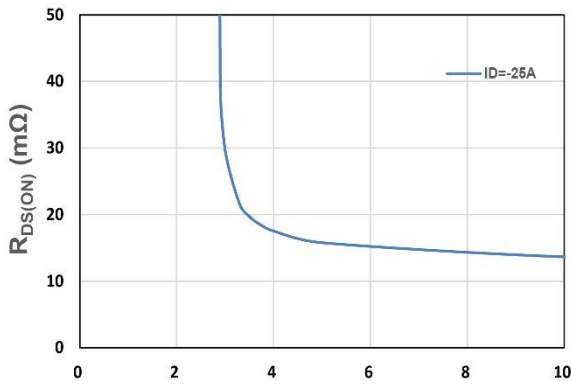


Figure 3. On-Resistance vs. VGS

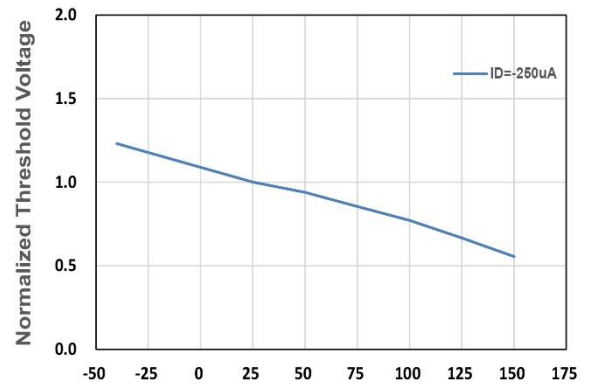


Figure 4. Gate Threshold Voltage

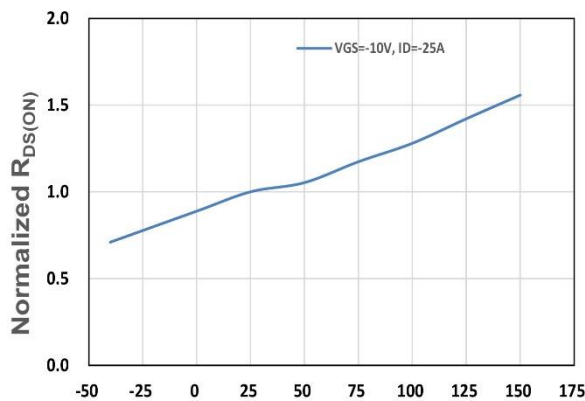


Figure 5. Drain-Source On Resistance

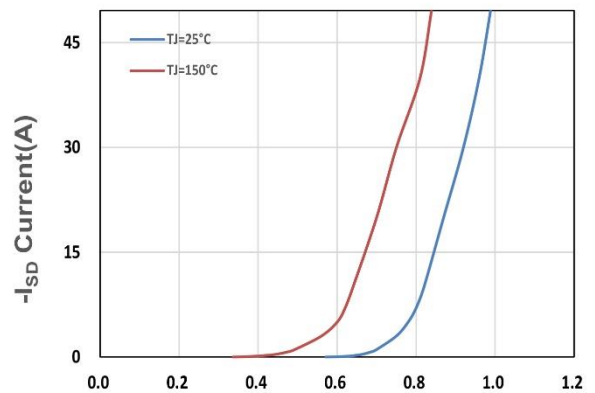
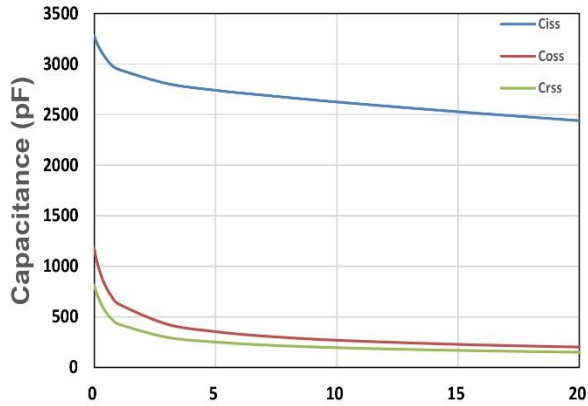
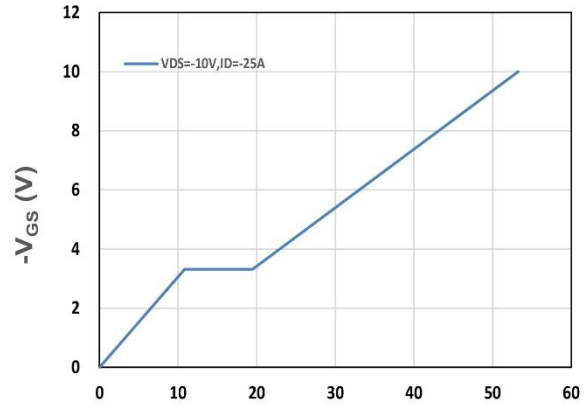


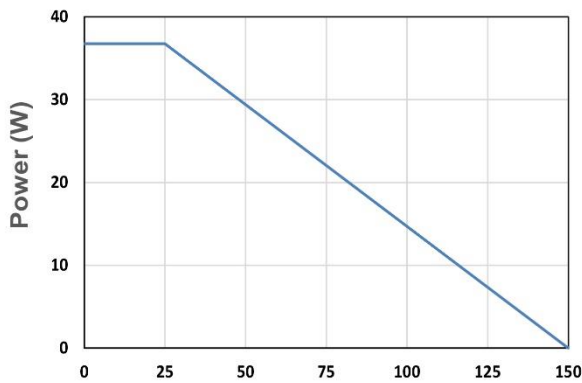
Figure 6. Source-Drain Diode Forward



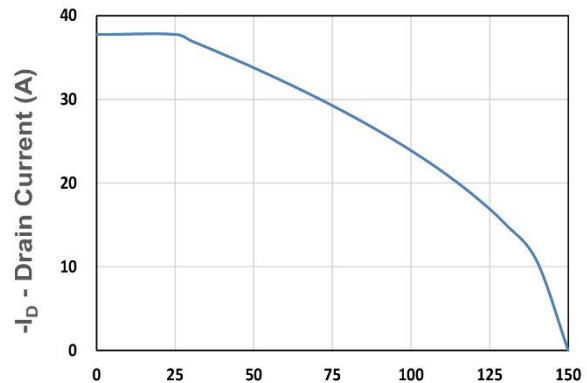
$-V_{DS}$ - Drain - Source Voltage (V)
Figure 7. Capacitance



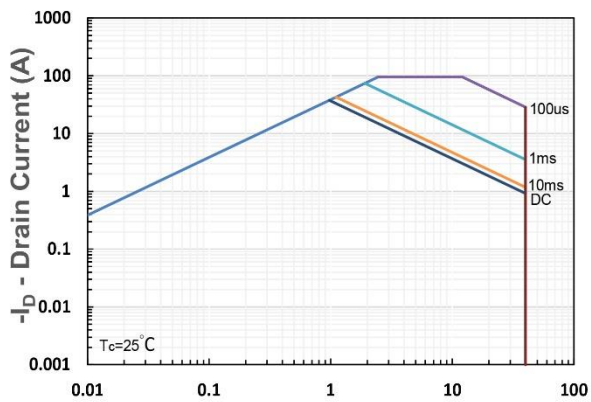
Q_g , Total Gate Charge (nC)
Figure 8. Gate Charge Characteristics



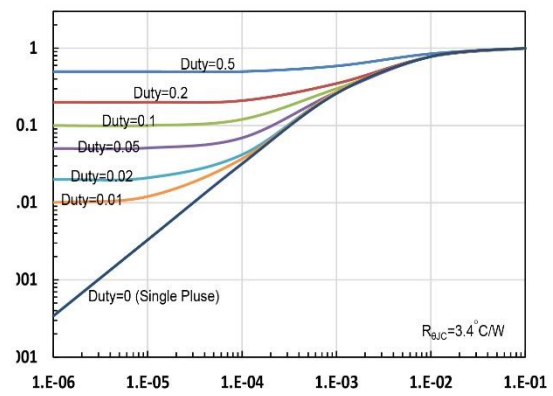
T_c - Case Temperature (°C)
Figure 9. Power Dissipation



T_c - Case Temperature (°C)
Figure 10. Drain Current



$-V_{DS}$ - Drain-Source Voltage (V)
Figure 11. Safe Operating Area



t_1 , Square Wave Pulse Duration (s)
Figure 12. $R_{\theta jC}$ Transient Thermal Impedance