



# Power MOSFETS

## DATASHEET

**LM40350PAP3A**

P-Channel  
Enhancement Mode MOSFET

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Quality Management Systems  
ISO 9001:2015 Certificate

## P-Channel Enhancement Mode MOSFET

### Pin Description

TO-220-3L (TOP view)	Symbol	Symbol	P-Channel	Unit
		$V_{DSS}$	-40	V
		$R_{DS(ON)-Max}$	33	$m\Omega$
		ID	-25	A

### Feature

- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- 100% UIS Tested

### Applications

- Load switches
- Synchronous Rectification

### Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM40350PAP3A	TO-220-3L	Tube	50 / Tape & Reel	40350 <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>

### Absolute Maximum Ratings ( $T_J=25^\circ C$ Unless Otherwise Noted)

Symbol	Parameter	P-Channel	Unit
$V_{DSS}$	Drain-Source Voltage	-40	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	
$T_J$	Maximum Junction Temperature	150	$^\circ C$
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$I_{DM}^{①}$	Pulse Drain Current Tested	$T_c=25^\circ C$	A
$I_D$	Continuous Drain Current	$T_c=25^\circ C$	-25
		$T_c=100^\circ C$	-16
$P_D$	Maximum Power Dissipation	$T_c=25^\circ C$	38
		$T_c=100^\circ C$	15
$I_{AS}^{②}$	Avalanche Current, Single pulse	L=0.1mH	A
$E_{AS}^{②}$	Avalanche Energy, Single pulse	L=0.1mH	12.8
			mJ

### Thermal Characteristics

Symbol	Parameter	Rating	Unit
$R_{θJC}$	Thermal Resistance-Junction to Case	Steady State	3.3
$R_{θJA}^{③}$	Thermal Resistance-Junction to Ambient	Steady State	62.5

Note ① : Max. current is limited by bonding wire

Note ② : UIS tested and pulse width are limited by maximum junction temperature  $150^\circ C$

Note ③ : Surface Mounted on 1in<sup>2</sup> FR-4 board with 1oz.

P-Channel Electrical Characteristics ( $T_J=25^\circ\text{C}$  Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static Electrical Characteristics</b>						
$\mathbf{BV_{DSS}}$	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}, I_{DS}=-250\mu\text{A}$	-40	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=-32\text{V}, V_{GS}=0\text{V}$	-	-	-1	$\mu\text{A}$
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_{DS}=-250\mu\text{A}$	-1	-1.7	-2.5	V
$I_{GSS}$	Gate Leakage Current	$V_{GS}=\pm 20\text{V}, V_{DS}=0\text{V}$	-	-	$\pm 100$	$\text{nA}$
$R_{DS(\text{ON})}^{\text{(4)}}$	Drain-Source On-state Resistance	$V_{GS}=-10\text{V}, I_{DS}=-10\text{A}$	-	28	34	$\text{m}\Omega$
		$V_{GS}=-4.5\text{V}, I_{DS}=-5\text{A}$	-	33	43	
$g_{fs}$	Forward Transconductance	$V_{DS}=-5\text{V}, I_{DS}=-5\text{A}$	-	14.5	-	S
<b>Dynamic Characteristics <sup>(5)</sup></b>						
$R_G$	Gate Resistance	$V_{GS}=0\text{V}, V_{DS}=0\text{V},$ $\text{Freq.}=1\text{MHz}$	-	11	-	$\Omega$
$C_{iss}$	Input Capacitance	$V_{GS}=0\text{V},$ $V_{DS}=-20\text{V},$ $\text{Freq.}=1\text{MHz}$	-	1316	-	$\text{pF}$
$C_{oss}$	Output Capacitance		-	102	-	
$C_{rss}$	Reverse Transfer Capacitance		-	78	-	
$t_{d(\text{ON})}$	Turn-on Delay Time	$V_{GS}=-10\text{V}, V_{DS}=-30\text{V},$ $I_D=-1\text{A}, R_{\text{GEN}}=6\Omega$	-	4.8	-	$\text{nS}$
$t_r$	Turn-on Rise Time		-	17.6	-	
$t_{d(\text{OFF})}$	Turn-off Delay Time		-	88.5	-	
$t_f$	Turn-off Fall Time		-	48.8	-	
$Q_g$	Total Gate Charge	$V_{GS}=-4.5\text{V}, V_{DS}=-20\text{V}$ $I_D=-10\text{A}$	-	13	-	$\text{nC}$
$Q_g$	Total Gate Charge	$V_{GS}=-10\text{V}, V_{DS}=-20\text{V},$ $I_D=-10\text{A}$	-	26.9	-	
$Q_{gs}$	Gate-Source Charge		-	4.88	-	
$Q_{gd}$	Gate-Drain Charge		-	4.51	-	
<b>Source-Drain Characteristics</b>						
$V_{SD}^{\text{(4)}}$	Diode Forward Voltage	$I_{SD}=-5\text{A}, V_{GS}=0\text{V}$	-	-0.8	-1.1	V
$t_{rr}$	Reverse Recovery Time	$I_F=-5\text{A}, V_R=-20\text{V}$	-	14.6	-	$\text{nS}$
$Q_{rr}$	Reverse Recovery Charge		-	7.2	-	$\text{nC}$

Note <sup>(4)</sup> : Pulse test (pulse width $\leq 300\text{us}$ , duty cycle $\leq 2\%$ ).Note <sup>(5)</sup> : Guaranteed by design, not subject to production testing.

## P-Channel Typical Characteristics

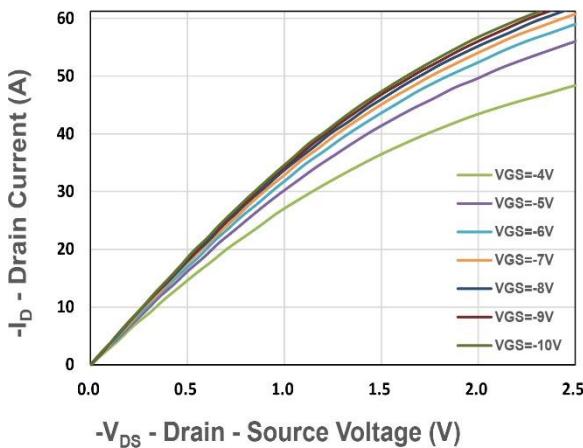


Figure 1. Output Characteristics

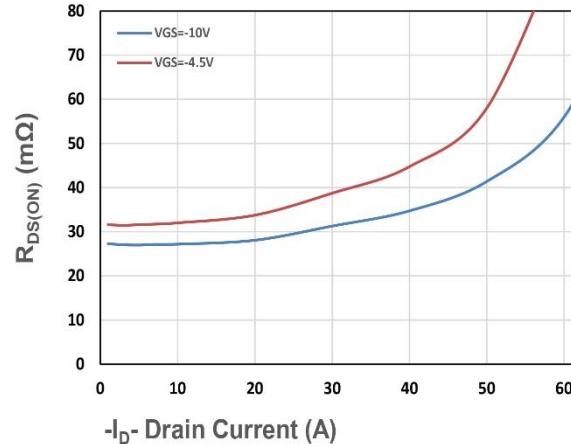


Figure 2. On-Resistance vs. ID

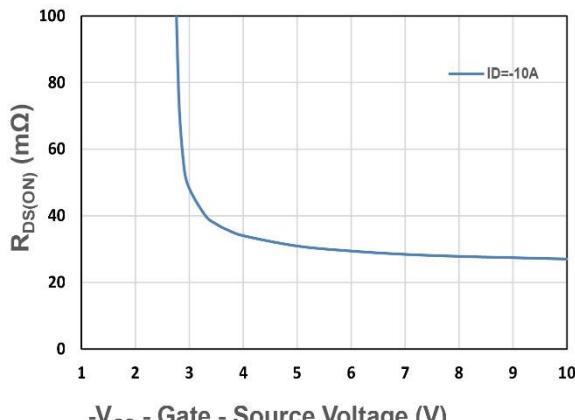


Figure 3. On-Resistance vs. VGS

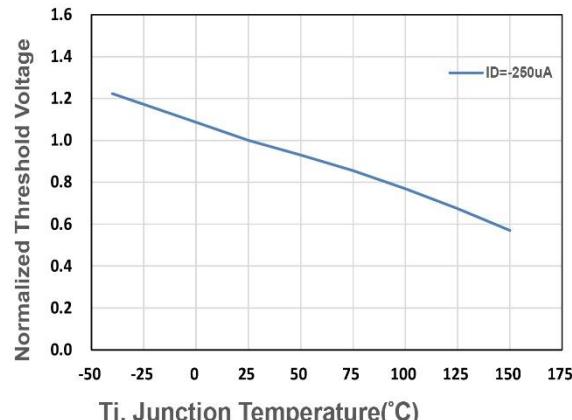


Figure 4. Gate Threshold Voltage

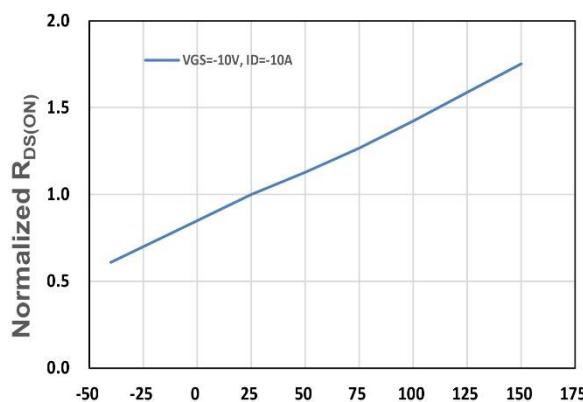


Figure 5. Drain-Source On Resistance

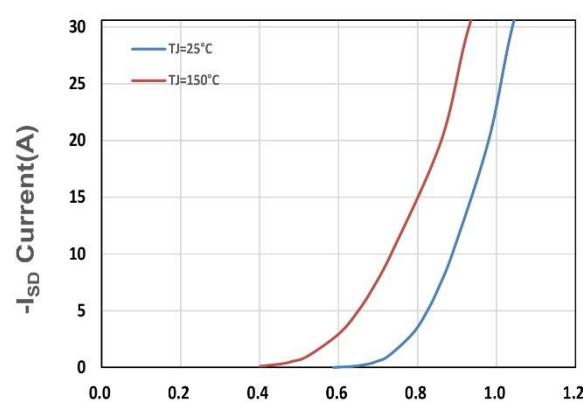
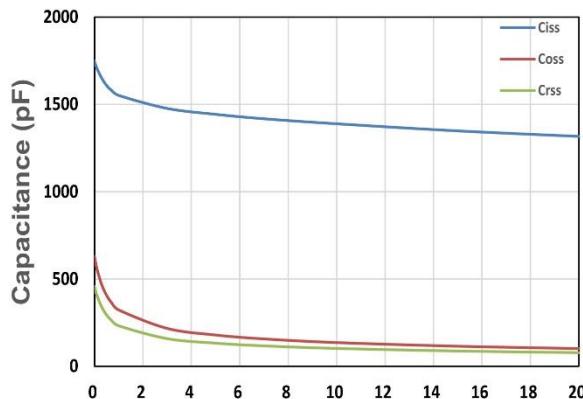
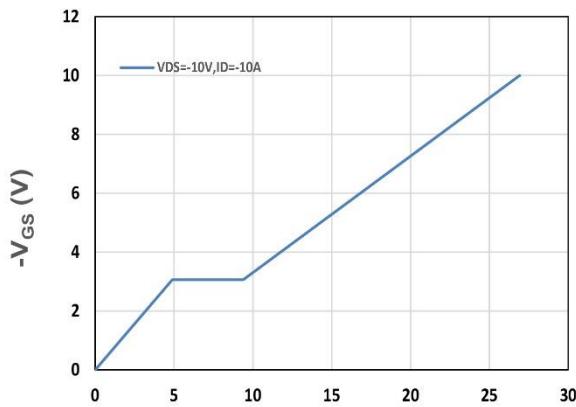


Figure 6. Source-Drain Diode Forward

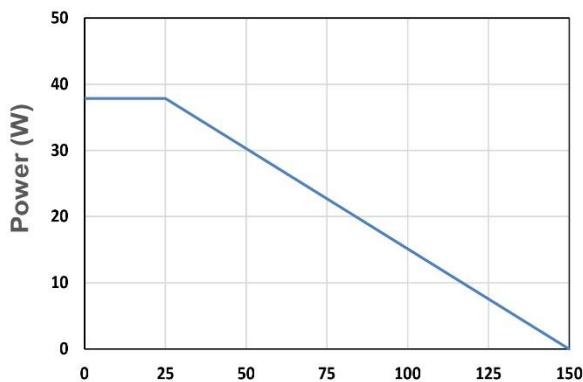
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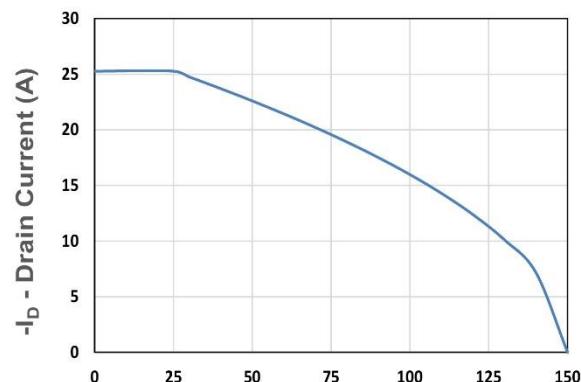
-V<sub>DS</sub> - Drain - Source Voltage (V)  
Figure 7. Capacitance



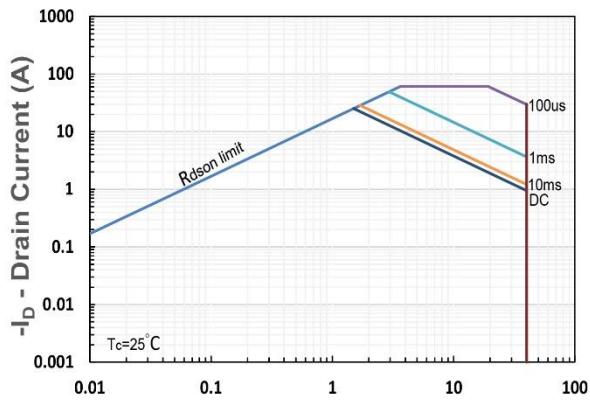
Q<sub>g</sub>, Total Gate Charge (nC)  
Figure 8. Gate Charge Characteristics



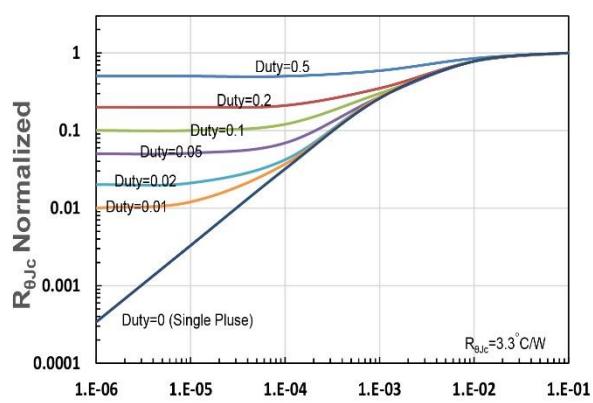
T<sub>c</sub> - Case Temperature (°C)  
Figure 9. Power Dissipation



T<sub>c</sub> - Case Temperature (°C)  
Figure 10. Drain Current



-V<sub>DS</sub> - Drain-Source Voltage (V)  
Figure 11. Safe Operating Area



t<sub>1</sub>, Square Wave Pulse Duration(s)  
Figure 12. R<sub>θJC</sub> Transient Thermal Impedance