




Power MOSFETS


DATASHEET

LM60026NAK8A

N-Channel
Enhancement Mode MOSFET

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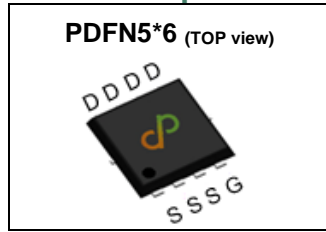


Quality Management Systems

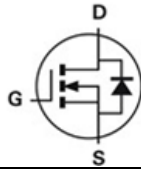
ISO 9001:2015 Certificate

N-Channel Enhancement Mode MOSFET

Pin Description



Symbol



Product Summary

Symbol	N-Channel	Unit
V_{DSS}	60	V
$R_{DS(ON)-Max}$	2.6	m Ω
I_D	142	A

Feature

- Optimized high performance of R_{on} and Q_g
- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- 100% UIS and Rg Tested

Applications

- DC-DC Converter
- Load Switching

Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM60026NAK8A	PDFN5*6	Tape & Reel	5000 / Tape & Reel	60026 □□□□□G

Absolute Maximum Ratings (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter	N-Channel	Unit
V_{DSS}	Drain-Source Voltage	60	V
V_{GSS}	Gate-Source Voltage	±20	
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-55 to 150	°C
$I_{DM}^{①}$	Pulse Drain Current Tested	$T_C=25^\circ C$ 142	A
I_D	Continuous Drain Current	$T_C=25^\circ C$ 142	A
		$T_C=100^\circ C$ 100	
P_D	Maximum Power Dissipation	$T_C=25^\circ C$ 96	W
		$T_C=100^\circ C$ 39	
$I_{AS}^{②}$	Avalanche Current, Single pulse	L=0.1mH 30	A
$E_{AS}^{③}$	Avalanche Energy, Single pulse	L=0.1mH 45	mJ

Thermal Characteristics

Symbol	Parameter	Rating	Unit
$R_{\theta JC}$	Thermal Resistance-Junction to Case	Steady State	1.3 °C/W
$R_{\theta JA}^{③}$	Thermal Resistance-Junction to Ambient	Steady State	50 °C/W

Note ① : Max. current is limited by bonding wire

Note ② : UIS tested and pulse width are limited by maximum junction temperature 150°C

Note ③ : Surface Mounted on 1in² FR-4 board with 1oz.

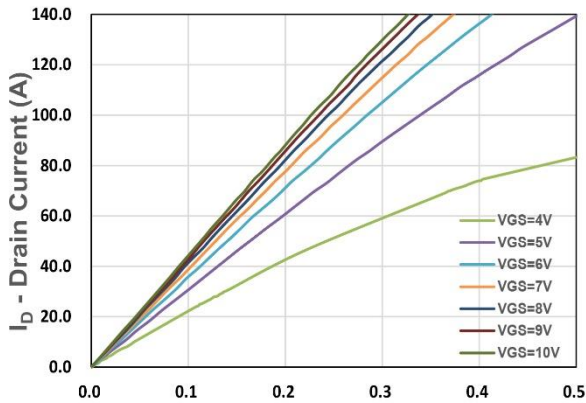
N-Channel Electrical Characteristics (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Electrical Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =250uA	60	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V _{DS} =48V, V _{GS} =0V	-	-	1	uA
V_{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =250uA	1	2	3	V
I_{GSS}	Gate Leakage Current	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
R_{DS(ON)}^④	Drain-Source On-state Resistance	V _{GS} =10V, I _{DS} =20A	-	2.2	2.6	mΩ
		V _{GS} =4.5V, I _{DS} =10A	-	3.5	4.5	
g_{fs}	Forward Transconductance	V _{DS} =5V, I _{DS} =20A	-	50	-	S
Dynamic Characteristics[®]						
R_G	Gate Resistance	V _{GS} =0V, V _{DS} =0V, Freq.=1MHz	-	1.7	-	Ω
C_{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =30V, Freq.=1MHz	-	4635	-	pF
C_{oss}	Output Capacitance					
C_{rss}	Reverse Transfer Capacitance					
t_{d(ON)}	Turn-on Delay Time	V _{GS} =10V, V _{DS} =30V, I _D =1A, R _{GEN} =6Ω	-	13.8	-	nS
t_r	Turn-on Rise Time					
t_{d(OFF)}	Turn-off Delay Time					
t_f	Turn-off Fall Time					
Q_g	Total Gate Charge	V _{GS} =4.5V, V _{DS} =30V, I _D =20A	-	39.5	-	nC
Q_g	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =20A	-	76.2	-	
Q_{gs}	Gate-Source Charge		-	13.4	-	
Q_{gd}	Gate-Drain Charge		-	17.5	-	
Source-Drain Characteristics						
V_{SD}^④	Diode Forward Voltage	I _{SD} =20A, V _{GS} =0V	-	0.8	1.1	V
t_{rr}	Reverse Recovery Time	I _F =20A, V _R =30V	-	27.6	-	nS
Q_{rr}	Reverse Recovery Charge	dI _F /dt=100A/μs	-	20.8	-	nC

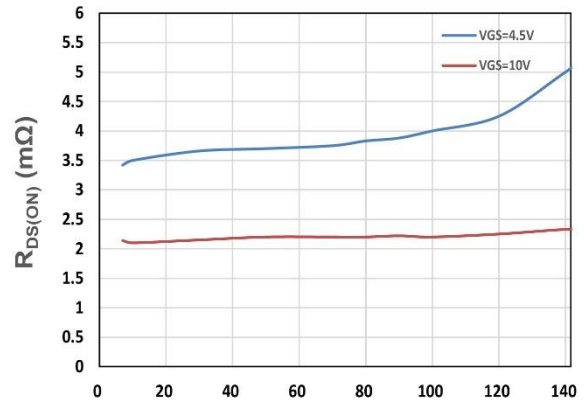
Note ④ : Pulse test (pulse width≤300us, duty cycle≤2%).

Note ⑤ : Guaranteed by design, not subject to production testing.

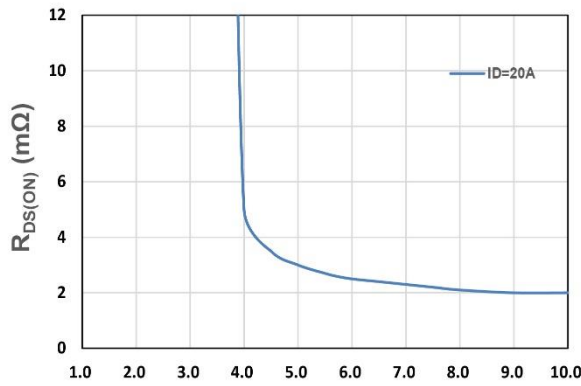
N-Channel Typical Characteristics



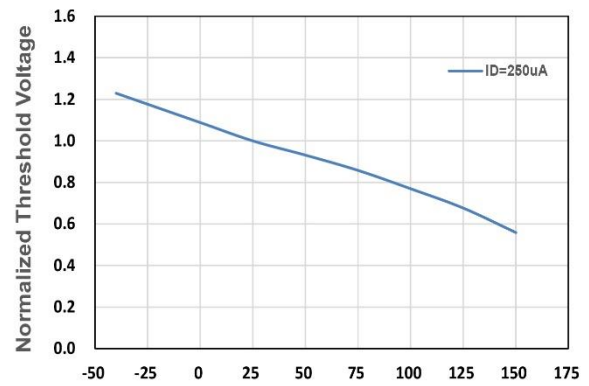
V_{DS} - Drain - Source Voltage (V)
Figure 1. Output Characteristics



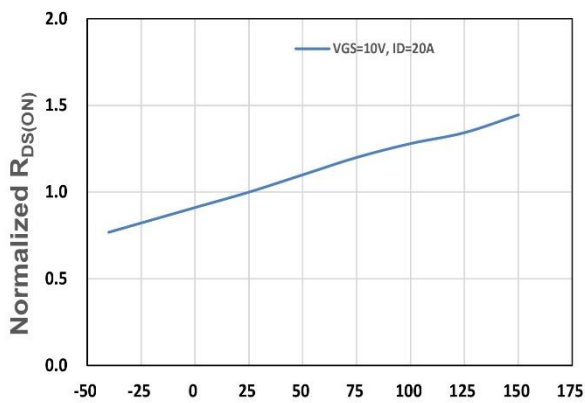
I_D - Drain Current (A)
Figure 2. On-Resistance vs. ID



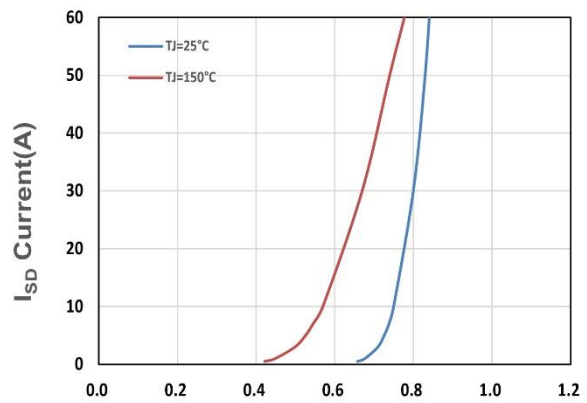
V_{GS} - Gate - Source Voltage (V)
Figure 3. On-Resistance vs. VGS



T_j , Junction Temperature($^{\circ}C$)
Figure 4. Gate Threshold Voltage



T_j , Junction Temperature($^{\circ}C$)
Figure 5. Drain-Source On Resistance



V_{SD} , Source-Drain Voltage(V)
Figure 6. Source-Drain Diode Forward

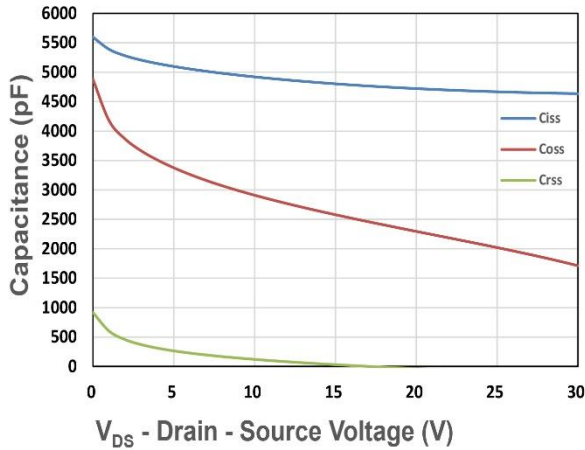


Figure 7. Capacitance

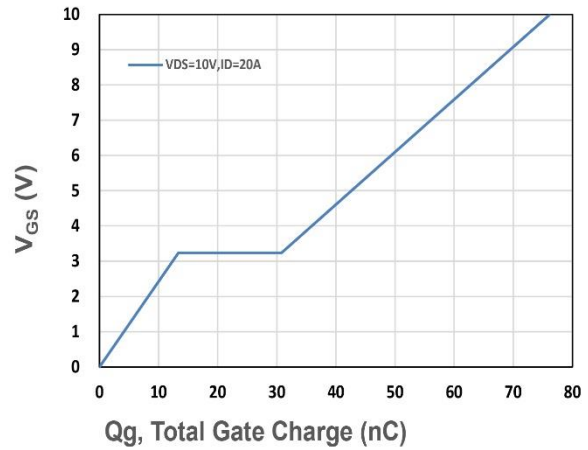


Figure 8. Gate Charge Characteristics

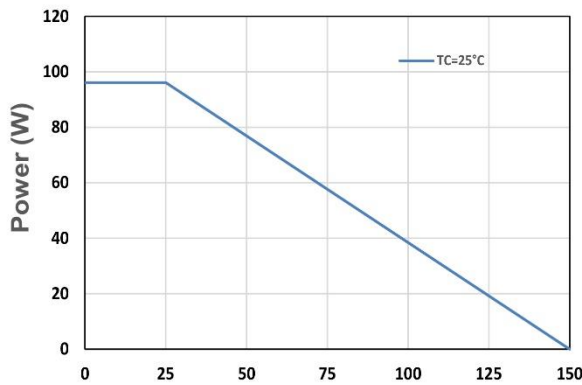


Figure 9. Power Dissipation

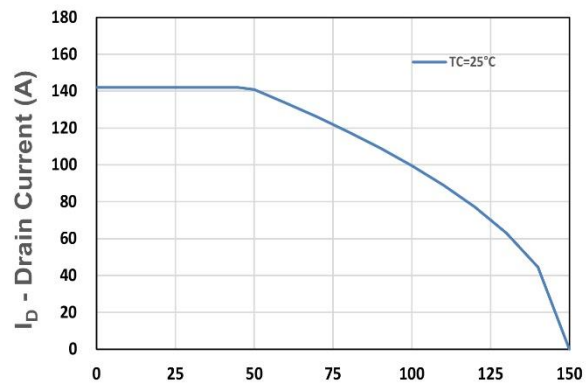


Figure 10. Drain Current

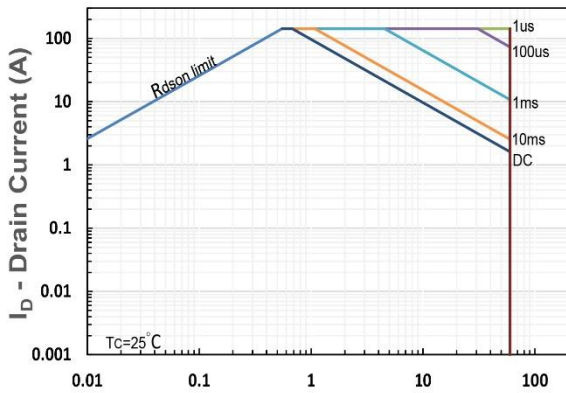


Figure 11. Safe Operating Area

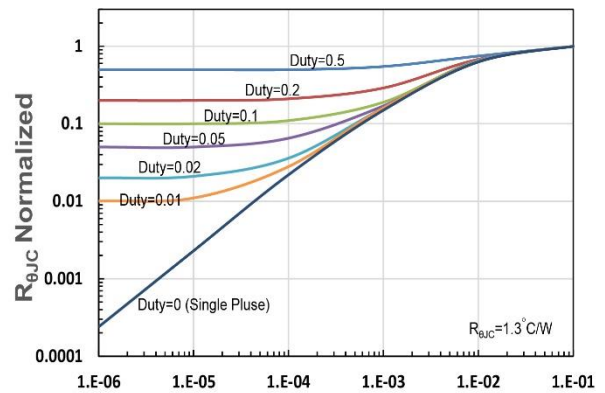


Figure 12. $R_{\theta JC}$ Transient Thermal Impedance