



# Power MOSFETS

## DATASHEET

**LM60M80PEI3A**

P-Channel  
Enhancement Mode MOSFET

-  Leadpower-semiconductor Corp., Ltd
-  sales@leadpower-semi.com
-  (03) 6577339 FAX : (03) 6577229
-  [www.leadpower-semi.com](http://www.leadpower-semi.com)



Quality Management Systems  
ISO 9001:2015 Certificate

## P-Channel Enhancement Mode MOSFET

### Pin Description

SOT-23 (TOP view)	Symbol	Symbol	P-Channel	Unit
		$V_{DSS}$	-60	V
		$R_{DS(ON)-Max}$	4.3	$\Omega$
		$I_D$	-0.21	A

### Feature

- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- ESD Protection

### Ordering Information

### Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM60M80PEI3A	SOT-23	Tape & Reel	3000 / Tape & Reel	12□□□

### Absolute Maximum Ratings ( $T_J=25^\circ\text{C}$ Unless Otherwise Noted)

Symbol	Parameter		P-Channel	Unit
$V_{DSS}$	Drain-Source Voltage		-60	V
$V_{GSS}$	Gate-Source Voltage		$\pm 20$	
$T_J$	Maximum Junction Temperature		150	$^\circ\text{C}$
$T_{STG}$	Storage Temperature Range		-55 to 150	$^\circ\text{C}$
$I_{DM}^{\text{(1)}}$	Pulse Drain Current Tested	$T_A=25^\circ\text{C}$	-0.53	A
$I_D$	Continuous Drain Current	$T_A=25^\circ\text{C}$	-0.21	A
		$T_A=70^\circ\text{C}$	-0.17	
$P_D$	Maximum Power Dissipation	$T_A=25^\circ\text{C}$	0.36	W
		$T_A=70^\circ\text{C}$	0.23	

### Thermal Characteristics

Symbol	Parameter		Rating	Unit
$R_{\text{JA}}^{\text{(3)}}$	Thermal Resistance-Junction to Ambient	Steady State	350	$^\circ\text{C/W}$

Note ① : Max. current is limited by junction temperature

Note ② : UIS tested and pulse width are limited by maximum junction temperature  $150^\circ\text{C}$

Note ③ : Surface Mounted on 1in<sup>2</sup> FR-4 board with 1oz.

# LM60M80PEI3A

## P-Channel Electrical Characteristics ( $T_J=25^\circ\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static Electrical Characteristics</b>						
$\text{BV}_{\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}$ , $I_{\text{DS}}=-250\mu\text{A}$	-60	-	-	V
$I_{\text{DSS}}$	Zero Gate Voltage Drain Current	$V_{\text{DS}}=-48\text{V}$ , $V_{\text{GS}}=0\text{V}$	-	-	-1	$\mu\text{A}$
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}$ , $I_{\text{DS}}=-250\mu\text{A}$	-1	-1.6	-2.5	V
$I_{\text{GSS}}$	Gate Leakage Current	$V_{\text{GS}}=\pm 20\text{V}$ , $V_{\text{DS}}=0\text{V}$	-	-	$\pm 10$	$\mu\text{A}$
$R_{\text{DS(ON)}}^{\circledast}$	Drain-Source On-state Resistance	$V_{\text{GS}}=-10\text{V}$ , $I_{\text{DS}}=-0.1\text{A}$	-	3.55	4.3	$\Omega$
		$V_{\text{GS}}=-4.5\text{V}$ , $I_{\text{DS}}=-0.1\text{A}$	-	3.8	5	
$g_{\text{fs}}$	Forward Transconductance	$V_{\text{DS}}=-5\text{V}$ , $I_{\text{DS}}=-0.1\text{A}$	-	4.4	-	S
<b>Dynamic Characteristics <sup>⑤</sup></b>						
$C_{\text{iss}}$	Input Capacitance	$V_{\text{GS}}=0\text{V}$ , $V_{\text{DS}}=-30\text{V}$ , Freq.=1MHz	-	30	-	pF
$C_{\text{oss}}$	Output Capacitance		-	12	-	
$C_{\text{rss}}$	Reverse Transfer Capacitance		-	6	-	
$t_{\text{d(ON)}}$	Turn-on Delay Time	$V_{\text{GS}}=-10\text{V}$ , $V_{\text{DS}}=-30\text{V}$ , $I_{\text{D}}=-1\text{A}$ , $R_{\text{GEN}}=6\Omega$	-	18.4	-	nS
$t_r$	Turn-on Rise Time		-	15.2	-	
$t_{\text{d(OFF)}}$	Turn-off Delay Time		-	113	-	
$t_f$	Turn-off Fall Time		-	41	-	
$Q_g$	Total Gate Charge	$V_{\text{GS}}=-4.5\text{V}$ , $V_{\text{DS}}=-30\text{V}$ $I_{\text{D}}=-0.37\text{A}$	-	0.47	-	nC
$Q_g$	Total Gate Charge	$V_{\text{GS}}=-10\text{V}$ , $V_{\text{DS}}=-30\text{V}$ , $I_{\text{D}}=-0.37\text{A}$	-	0.84	-	
$Q_{\text{gs}}$	Gate-Source Charge		-	0.19	-	
$Q_{\text{gd}}$	Gate-Drain Charge		-	0.21	-	
<b>Source-Drain Characteristics</b>						
$V_{\text{SD}}^{\circledast}$	Diode Forward Voltage	$I_{\text{SD}}=-0.1\text{A}$ , $V_{\text{GS}}=0\text{V}$	-	-0.8	-1.1	V
$t_{\text{rr}}$	Reverse Recovery Time	$I_F=-0.18\text{A}$ , $V_R=-30\text{V}$ $dI_F/dt=100\text{A}/\mu\text{s}$	-	10	-	nS
$Q_{\text{rr}}$	Reverse Recovery Charge		-	5	-	nC

Note ④ : Pulse test (pulse width $\leq 300\mu\text{s}$ , duty cycle $\leq 2\%$ ).

Note ⑤ : Guaranteed by design, not subject to production testing.

## P-Channel Typical Characteristics

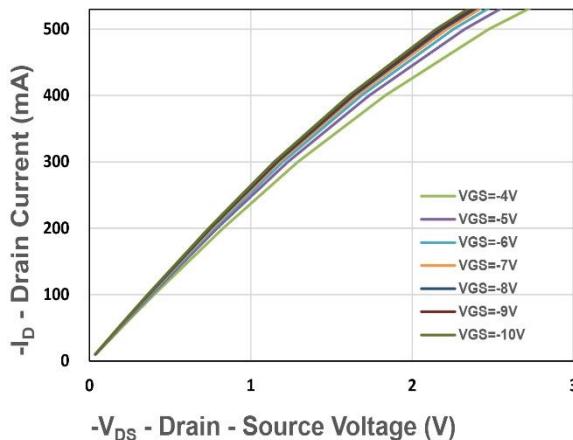


Figure 1. Output Characteristics

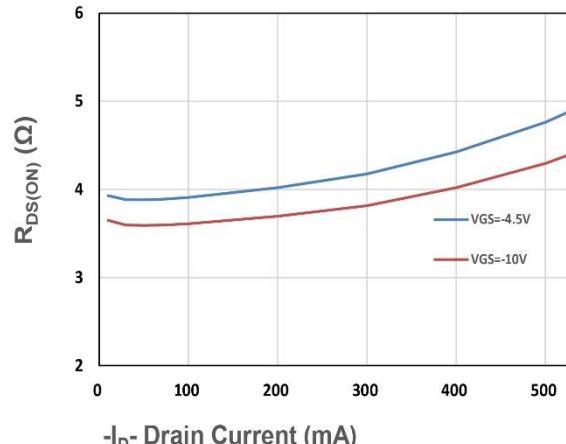


Figure 2. On-Resistance vs. ID

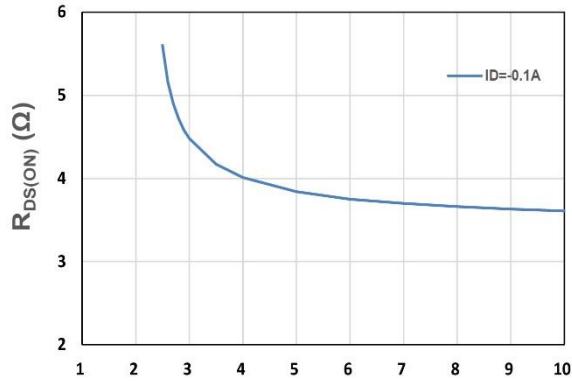


Figure 3. On-Resistance vs. VGS

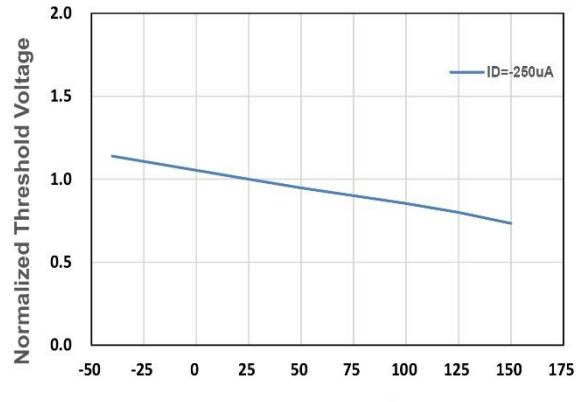


Figure 4. Gate Threshold Voltage

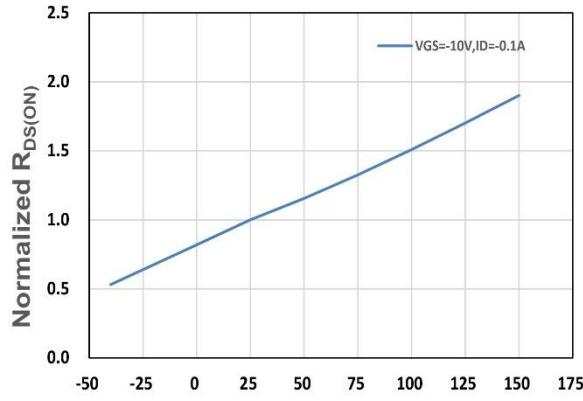


Figure 5. Drain-Source On Resistance

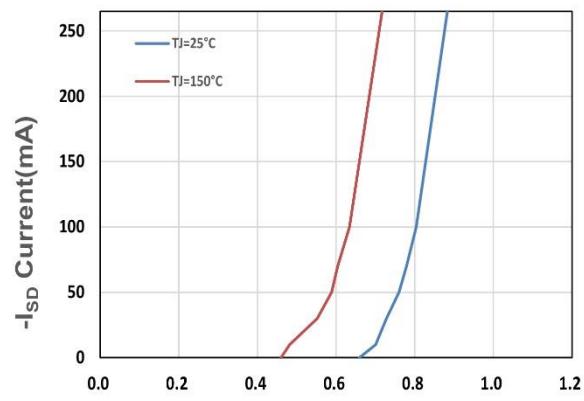
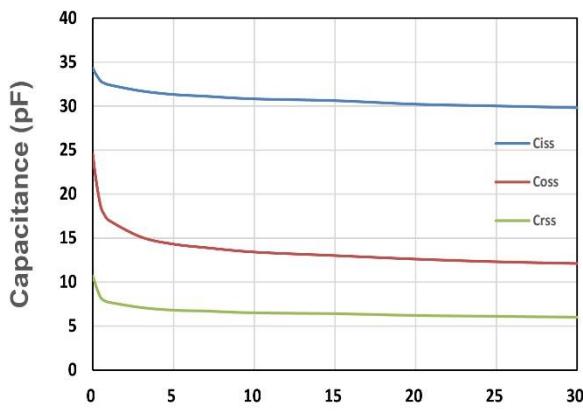
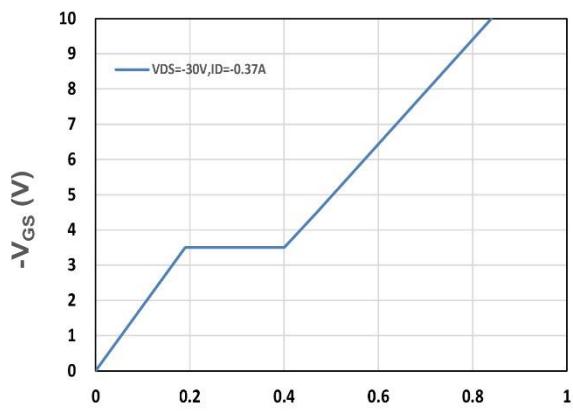


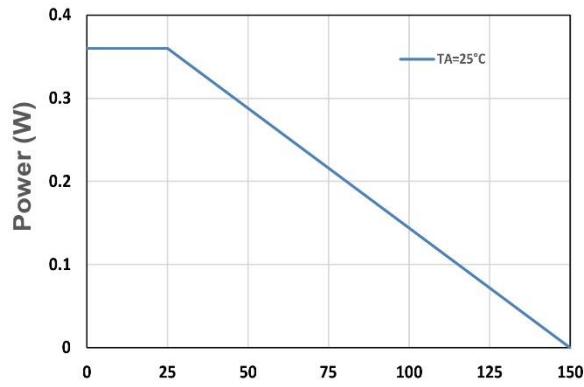
Figure 6. Source-Drain Diode Forward



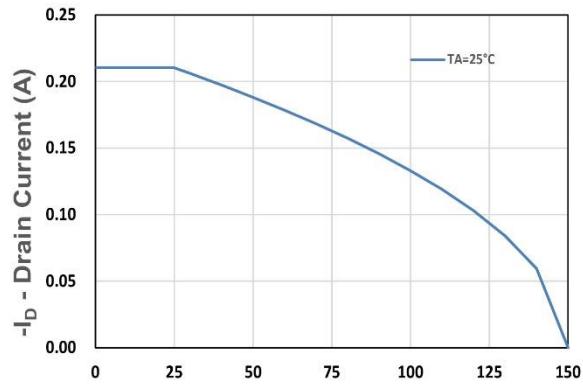
- $V_{DS}$  - Drain - Source Voltage (V)  
Figure 7. Capacitance



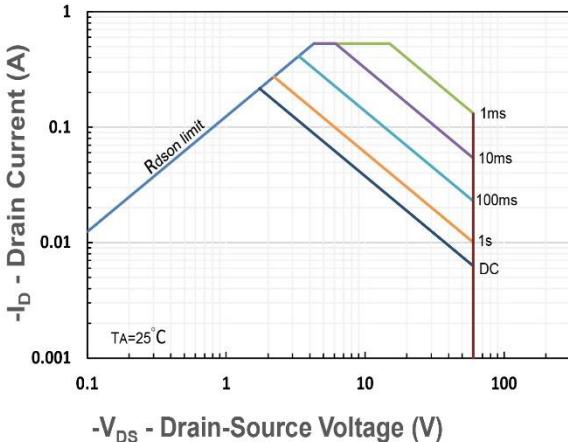
$Q_g$ , Total Gate Charge (nC)  
Figure 8. Gate Charge Characteristics



$T_j$  - Junction Temperature (°C)  
Figure 9. Power Dissipation

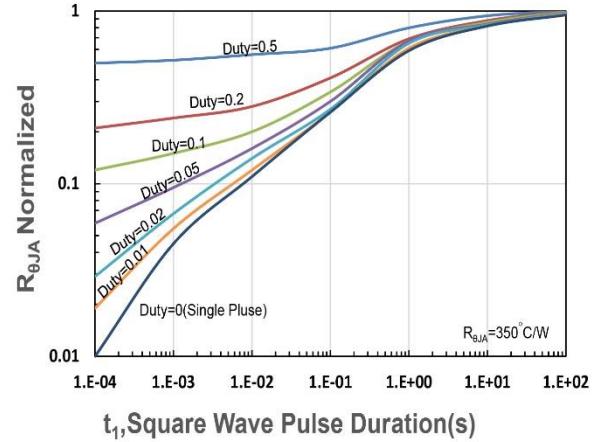


$-I_D$  - Drain Current (A)  
Figure 10. Drain Current



- $V_{DS}$  - Drain-Source Voltage (V)

Figure 11. Safe Operating Area



$R_{\theta JA}$  Normalized  
Figure 12.  $R_{\theta JA}$  Transient Thermal Impedance