



Power MOSFETS


DATASHEET

LM1F650NAQ8A

N-Channel
Enhancement Mode MOSFET

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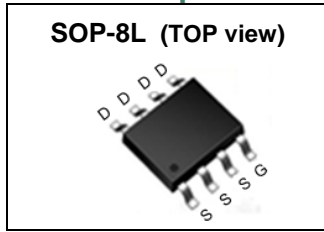


Quality Management Systems

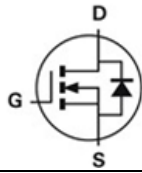
ISO 9001:2015 Certificate

N-Channel Enhancement Mode MOSFET

Pin Description



Symbol



Product Summary

Symbol	N-Channel	Unit
V_{DSS}	150	V
$R_{DS(ON)-Max}$	65	m Ω
I_D	3.3	A

Feature

- High Speed Power Switching
- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- 100% UIS Tested

Applications

- Synchronous Rectification in SMPS
- Hard Switching
- Telecoms and Industrial

Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM1F650NAQ8A	SOP-8L	Tape & Reel	3000 / Tape & Reel	1F650 □□□□□□

Absolute Maximum Ratings (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter	N-Channel	Unit	
V_{DSS}	Drain-Source Voltage	150	V	
V_{GSS}	Gate-Source Voltage	±20		
T_J	Maximum Junction Temperature	150	°C	
T_{STG}	Storage Temperature Range	-55 to 150	°C	
$I_{DM}^{①}$	Pulse Drain Current Tested	$T_A=25^\circ\text{C}$	8.3	A
I_D	Continuous Drain Current	$T_A=25^\circ\text{C}$	3.3	A
		$T_A=100^\circ\text{C}$	2.6	
P_D	Maximum Power Dissipation	$T_A=25^\circ\text{C}$	1.5	W
		$T_A=100^\circ\text{C}$	0.9	
$I_{AS}^{②}$	Avalanche Current, Single pulse	L=0.1mH	6	A
$E_{AS}^{②}$	Avalanche Energy, Single pulse	L=0.1mH	1.8	mJ

Thermal Characteristics

Symbol	Parameter	Rating	Unit	
$R_{\theta JA}^{③}$	Thermal Resistance-Junction to Ambient	Steady State	85	°C/W

Note ① : Max. current is limited by junction temperature

Note ② : UIS tested and pulse width are limited by maximum junction temperature 150°C

Note ③ : Surface Mounted on 1in² FR-4 board with 1oz.

N-Channel Electrical Characteristics (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Electrical Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =250uA	150	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V _{DS} =80V, V _{GS} =0V	-	-	1	uA
V_{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =250uA	1	2	3	V
I_{GSS}	Gate Leakage Current	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
R_{DS(ON)} ^④	Drain-Source On-state Resistance	V _{GS} =10V, I _{DS} =4A	-	54	65	mΩ
		V _{GS} =4.5V, I _{DS} =3A	-	62	82	
g_{fs}	Forward Transconductance	V _{DS} =5V, I _{DS} =2A	-	5.9	-	S
Dynamic Characteristics ^⑥						
R_G	Gate Resistance	V _{GS} =0V, V _{DS} =0V, Freq.=1MHz	-	2	-	Ω
C_{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =75V, Freq.=1MHz	-	643	-	pF
C_{oss}	Output Capacitance		-	50	-	
C_{rss}	Reverse Transfer Capacitance		-	15	-	
t_{d(ON)}	Turn-on Delay Time	V _{GS} =10V, V _{DS} =75V, I _D =1A, R _{GEN} =1Ω	-	6.2	-	nS
t_r	Turn-on Rise Time		-	2.3	-	
t_{d(OFF)}	Turn-off Delay Time		-	13.3	-	
t_f	Turn-off Fall Time		-	30.3	-	
Q_g	Total Gate Charge	V _{GS} =4.5V, V _{DS} =75V I _D =4A	-	5.3	-	nC
Q_g	Total Gate Charge	V _{GS} =10V, V _{DS} =75V, I _D =4A	-	10	-	
Q_{gs}	Gate-Source Charge		-	2.8	-	
Q_{gd}	Gate-Drain Charge		-	1.05	-	
Source-Drain Characteristics						
V_{SD} ^④	Diode Forward Voltage	I _{SD} =2A, V _{GS} =0V	-	0.8	1.1	V
t_{rr}	Reverse Recovery Time	I _F =2A, V _R =75V	-	42.5	-	nS
Q_{rr}	Reverse Recovery Charge	dI _F /dt=100A/μs	-	49.5	-	nC

Note ④ : Pulse test (pulse width≤300us, duty cycle≤2%).

Note ⑤ : Guaranteed by design, not subject to production testing.

N-Channel Typical Characteristics

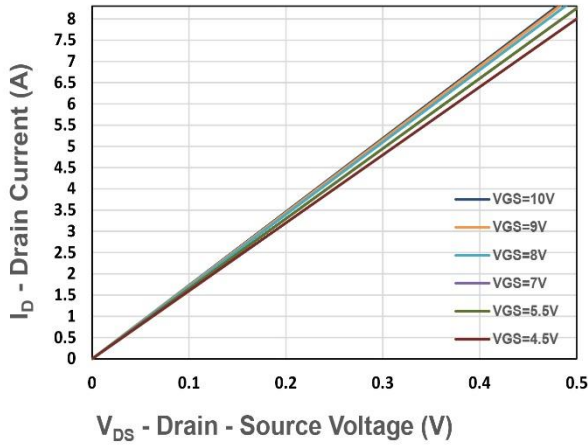


Figure 1. Output Characteristics

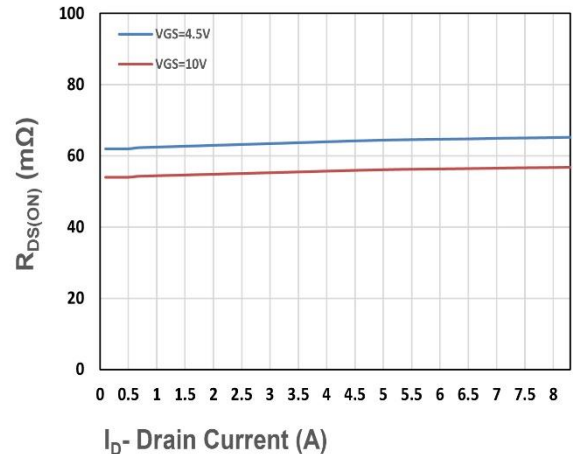


Figure 2. On-Resistance vs. ID

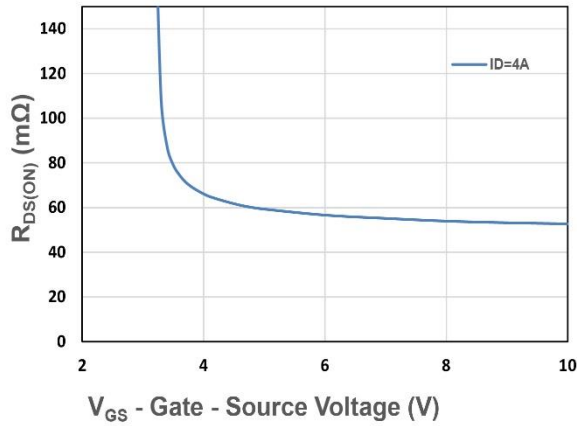


Figure 3. On-Resistance vs. VGS

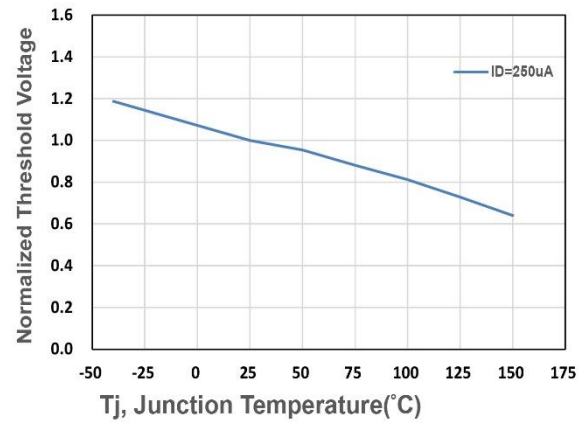


Figure 4. Gate Threshold Voltage

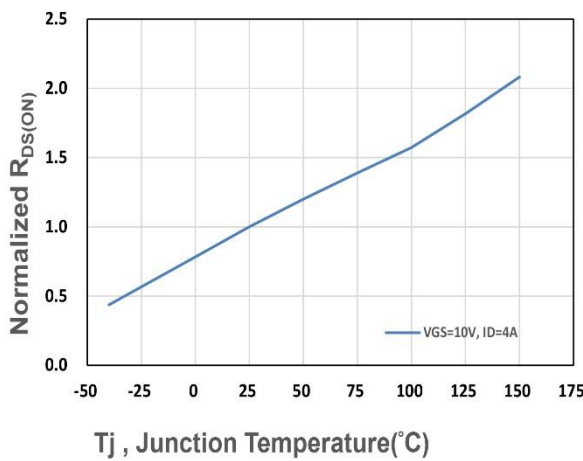


Figure 5. Drain-Source On Resistance

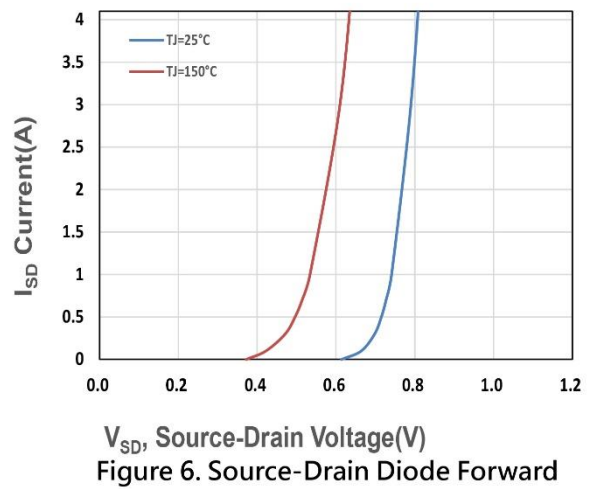
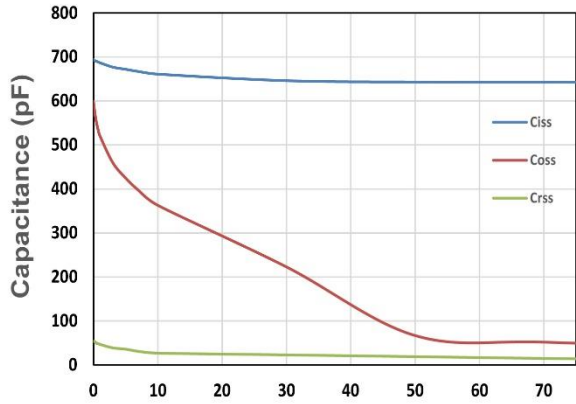
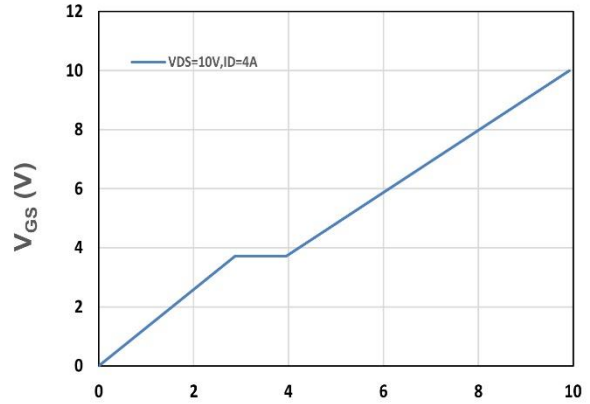


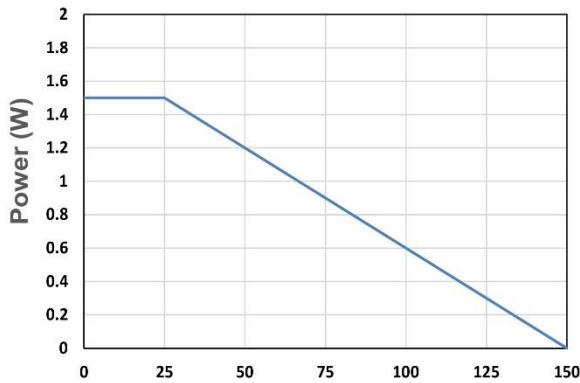
Figure 6. Source-Drain Diode Forward



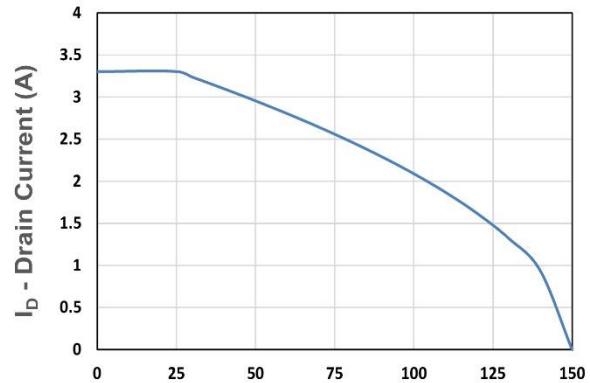
V_{DS} - Drain - Source Voltage (V)
Figure 7. Capacitance



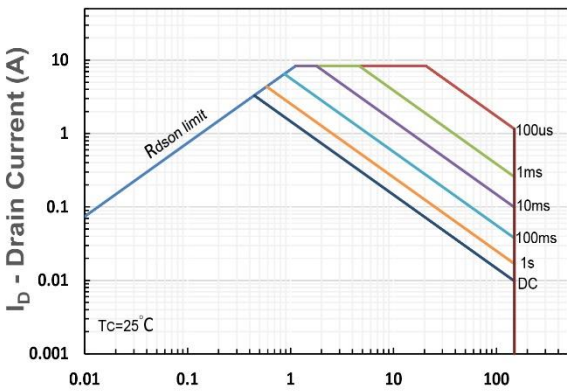
Q_g , Total Gate Charge (nC)
Figure 8. Gate Charge Characteristics



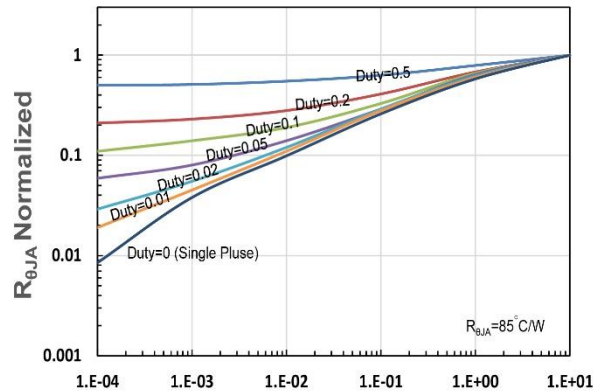
T_A - Ambient Temperature (°C)
Figure 9. Power Dissipation



T_A - Ambient Temperature (°C)
Figure 10. Drain Current



V_{DS} - Drain-Source Voltage (V)
Figure 11. Safe Operating Area



t_1 , Square Wave Pulse Duration(s)
Figure 12. $R_{\theta JA}$ Transient Thermal Impedance