




# Power MOSFETS


## DATASHEET


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**LM4435PAQ8A**

P-Channel  
Enhancement Mode MOSFET

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Quality Management Systems

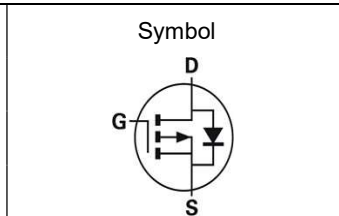
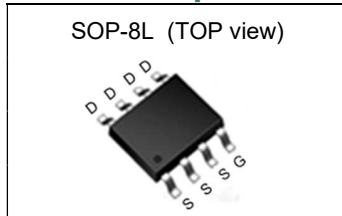
ISO 9001:2015 Certificate

# LM4435PAQ8A



## P-Channel Enhancement Mode MOSFET

### Pin Description



### Ordering Information

Symbol	P-Channel	Unit
$V_{DSS}$	<b>-30</b>	<b>V</b>
$R_{DS(ON)-Max}$	<b>14.5</b>	<b>mΩ</b>
$I_D$	<b>-8.4</b>	<b>A</b>

### Feature

- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- Lower  $Q_g$  and  $Q_{gd}$  for high-speed switching
- Lower  $R_{DS(ON)}$  to Minimize Conduction Losses
- 100% UIS Tested

### Applications

- Power Management in DC/DC
- Power Load Switch

### Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM4435PAQ8A	SOP-8L	Tape & Reel	3000 / Tape & Reel	4435 □□□□□□

Note : □□□□□□ = Lot Code

### Absolute Maximum Ratings ( $T_J=25^\circ\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	P-Channel	Unit
$V_{DSS}$	Drain-Source Voltage	-30	V
$V_{GSS}$	Gate-Source Voltage	$\pm 25$	
$T_J$	Maximum Junction Temperature	150	$^\circ\text{C}$
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$I_{DM}^{(1)}$	Pulse Drain Current Tested	$T_A=25^\circ\text{C}$	A
$I_D^{(2)}$	Continuous Drain Current	$T_A=25^\circ\text{C}$	-8.4
		$T_A=70^\circ\text{C}$	-6.7
$P_D^{(3)}$	Maximum Power Dissipation	$T_A=25^\circ\text{C}$	1.6
		$T_A=70^\circ\text{C}$	1
$I_{AS}^{(3)}$	Avalanche Current, Single pulse	L=0.1mH	-26
$E_{AS}^{(3)}$	Avalanche Energy, Single pulse	L=0.1mH	34

### Thermal Characteristics

Symbol	Parameter	Rating	Unit
$R_{\theta JA}^{(3)}$	Thermal Resistance-Junction to Ambient	$t \leq 10s$	40
		Steady State	80

Note ① : Max. current is limited by junction temperature.

Note ② : UIS tested and pulse width are limited by maximum junction temperature  $150^\circ\text{C}$

Note ③ : Surface Mounted on  $1\text{in}^2$  FR-4 board with 1oz.

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## P-Channel Electrical Characteristics (T<sub>J</sub>=25°C Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static Electrical Characteristics</b>						
<b>BV<sub>DSS</sub></b>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>DS</sub> =-250uA	-30	-	-	V
<b>I<sub>DSS</sub></b>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-24V, V <sub>GS</sub> =0V	-	-	-1	uA
<b>V<sub>GS(th)</sub></b>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>DS</sub> =-250uA	-1	-1.5	-2	V
<b>I<sub>GSS</sub></b>	Gate Leakage Current	V <sub>GS</sub> =±25V, V <sub>DS</sub> =0V	-	-	±100	nA
<b>R<sub>DS(ON)</sub></b> <sup>④</sup>	Drain-Source On-state Resistance	V <sub>GS</sub> =-10V, I <sub>DS</sub> =-10A	-	12	14.5	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>DS</sub> =-7A	-	15.5	20	
<b>gfs</b>	Forward Transconductance	V <sub>DS</sub> =-10V, I <sub>DS</sub> =-5A	-	14.7	-	S
<b>Dynamic Characteristics</b> <sup>⑤</sup>						
<b>R<sub>G</sub></b>	Gate Resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, Freq.=1MHz	-	8.9	-	Ω
<b>C<sub>iss</sub></b>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =-15V, Freq.=1MHz	-	2157	-	pF
<b>C<sub>oss</sub></b>	Output Capacitance		-	235	-	
<b>C<sub>rss</sub></b>	Reverse Transfer Capacitance		-	206	-	
<b>t<sub>d(ON)</sub></b>	Turn-on Delay Time	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-15V, I <sub>D</sub> =-20A, R <sub>GEN</sub> =3.3Ω	-	10.6	-	nS
<b>t<sub>r</sub></b>	Turn-on Rise Time		-	15.6	-	
<b>t<sub>d(OFF)</sub></b>	Turn-off Delay Time		-	90	-	
<b>t<sub>f</sub></b>	Turn-off Fall Time		-	31.2	-	
<b>Q<sub>g</sub></b>	Total Gate Charge	V <sub>GS</sub> =-4.5V, V <sub>DS</sub> =-15V, I <sub>D</sub> =-20A	-	23	-	nC
<b>Q<sub>g</sub></b>	Total Gate Charge	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-15V, I <sub>D</sub> =-20A	-	46	-	
<b>Q<sub>gs</sub></b>	Gate-Source Charge		-	6.5	-	
<b>Q<sub>gd</sub></b>	Gate-Drain Charge		-	8.8	-	
<b>Source-Drain Characteristics</b>						
<b>V<sub>SD</sub></b> <sup>④</sup>	Diode Forward Voltage	I <sub>SD</sub> =-3A, V <sub>GS</sub> =0V	-	-0.75	-1.1	V
<b>t<sub>rr</sub></b>	Reverse Recovery Time	I <sub>F</sub> =-10A, V <sub>R</sub> =-15V,	-	13.4	-	nS
<b>Q<sub>rr</sub></b>	Reverse Recovery Charge	dI <sub>F</sub> /dt=1A/μs	-	7.1	-	nC

Note ④ : Pulse test (pulse width≤300us, duty cycle≤2%).

Note ⑤ : Guaranteed by design, not subject to production testing.

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## P-Channel Typical Characteristics

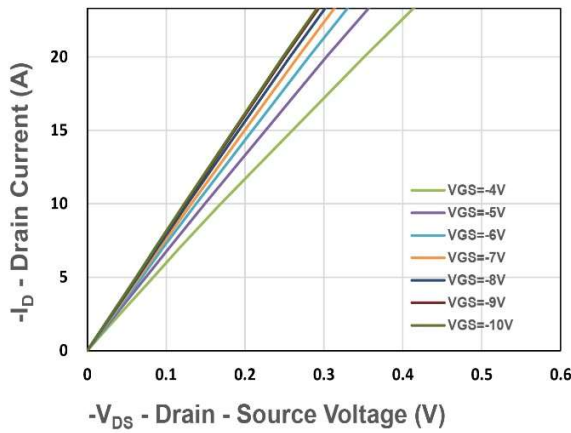


Figure 1. Output Characteristics

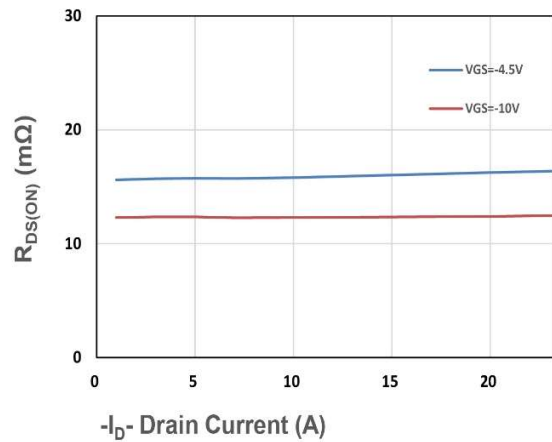


Figure 2. On-Resistance vs. ID

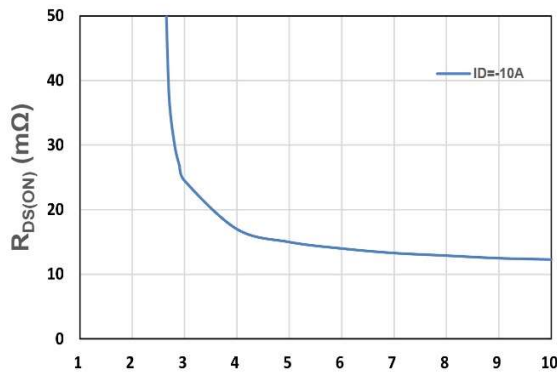


Figure 3. On-Resistance vs. VGS

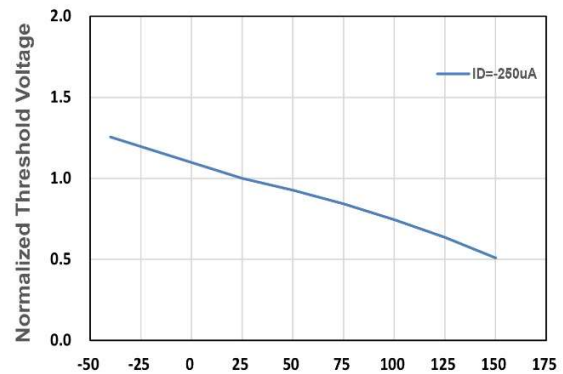


Figure 4. Gate Threshold Voltage

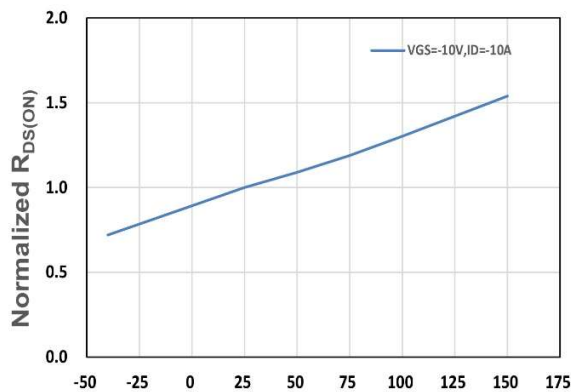


Figure 5. Drain-Source On Resistance

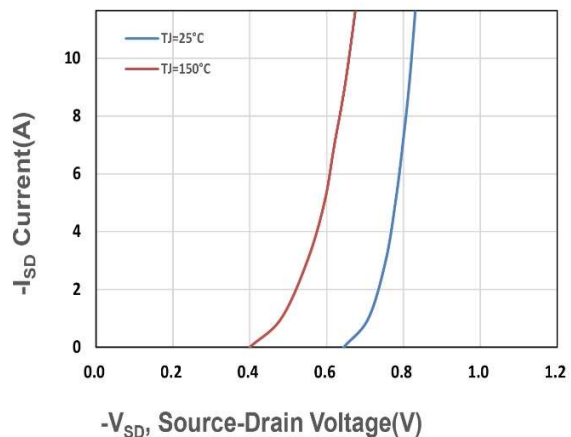
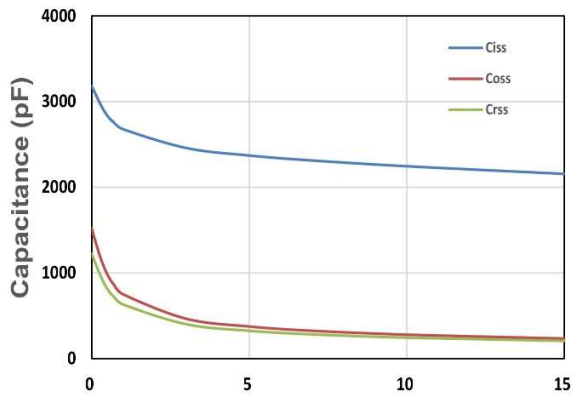
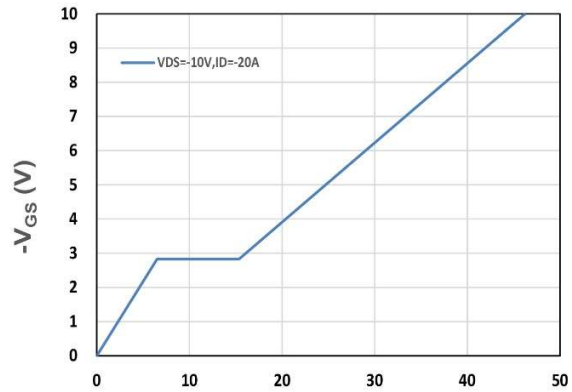


Figure 6. Source-Drain Diode Forward

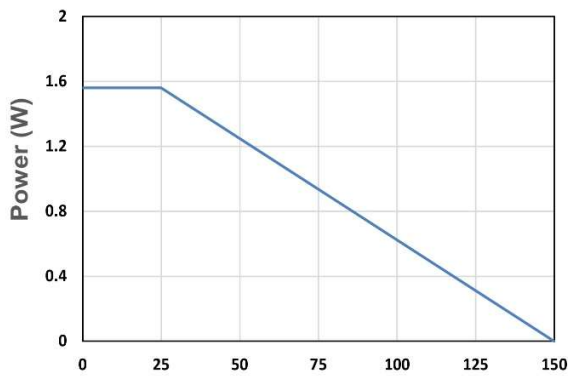
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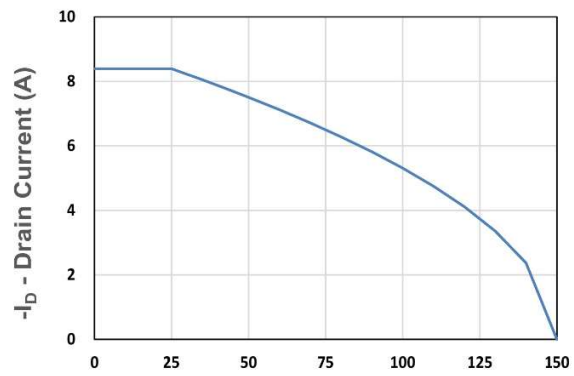
$-V_{DS}$  - Drain - Source Voltage (V)  
Figure 7. Capacitance



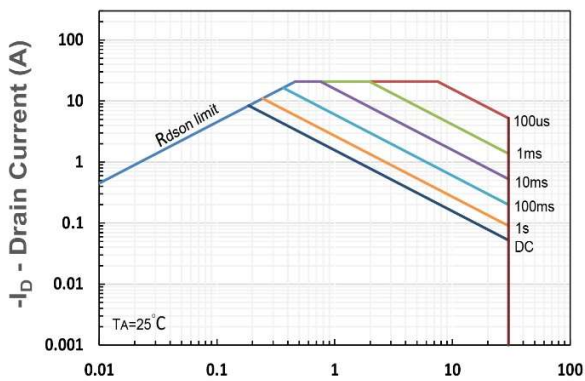
$Q_g$ , Total Gate Charge (nC)  
Figure 8. Gate Charge Characteristics



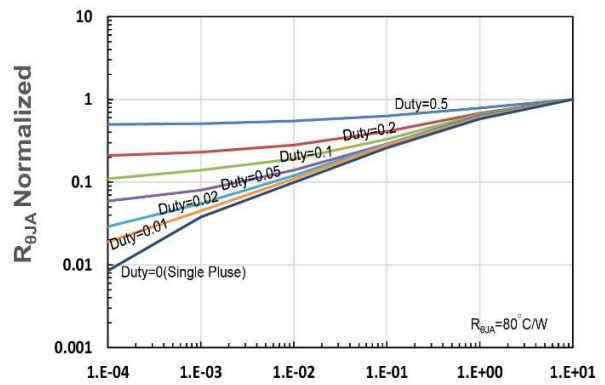
$T_A$  - Ambient Temperature (°C)  
Figure 9. Power Dissipation



$T_A$  - Ambient Temperature (°C)  
Figure 10. Drain Current



$-V_{DS}$  - Drain-Source Voltage (V)  
Figure 11. Safe Operating Area



$t_1$ , Square Wave Pulse Duration (s)  
Figure 12.  $R_{\theta JA}$  Transient Thermal Impedance