Power MOSFETS

DATASHEET

LM20A12PLQ8A

P-Channel

Enhancement Mode MOSFET

Leadpower-semiconductor Corp., Ltd

sales@leadpower-semi.com

(03) 6577339 FAX：(03) 6577229

www.leadpower-semi.com

Quality Management Systems

ISO 9001:2015 Certificate

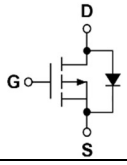
LM20A12PLQ8A

P-Channel Enhancement Mode MOSFET

Pin Description

SOP-8L (TOP view)

Symbol



Ordering Information

Symbol	P-Channel	Unit
V_{DSS}	-20	V
$R_{DS(ON)-Max}$	112	mΩ
I_D	-2.7	A

Feature

- Lower Q_g and Q_{gd}
- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- 100% UIS Tested

Applications

- Portable Equipment
- Battery Powered System

Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM20A12PLQ8A	SOP-8L	Tape & Reel	3000 / Tape & Reel	20A12 □□□□□□

Note：□□□□□□ = Lot Code

Absolute Maximum Ratings (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter		P-Channel	Unit
V_{DSS}	Drain-Source Voltage		-20	V
V_{GSS}	Gate-Source Voltage		±12	
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature Range		-55 to 150	°C
I_{DM}①	Pulse Drain Current Tested	T_A=25°C	-6.6	A
I_D	Continuous Drain Current	T_A=25°C	-2.7	A
		T_A=70°C	-2.1	
P_D	Maximum Power Dissipation	T_A=25°C	1.3	W
		T_A=70°C	0.8	
I_{AS}②	Avalanche Current, Single pulse	L=0.1mH	-11.8	A
E_{AS}②	Avalanche Energy, Single pulse	L=0.1mH	7	mJ

Thermal Characteristics

Symbol	Parameter		Rating	Unit
$R_{\theta JA}$③	Thermal Resistance-Junction to Ambient	Steady State	100	°C/W

Note ①：Max. current is limited by junction temperature.
Note ②：UIS tested and pulse width are limited by maximum junction temperature 150°C
Note ③：Surface Mounted on 1in² FR-4 board with 1oz.

P-Channel Electrical Characteristics (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Electrical Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_{DS}=-250uA	-20	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-16V, V_{GS}=0V	-	-	-1	uA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_{DS}=-250uA	-0.35	-0.6	-1	V
I_{GSS}	Gate Leakage Current	V_{GS}=±12V, V_{DS}=0V	-	-	±100	nA
$R_{DS(ON)}$④	Drain-Source On-state Resistance	V_{GS}=-4.5V, I_{DS}=-1.5A	-	95	112	mΩ
		V_{GS}=-2.5V, I_{DS}=-1.5A	-	124	161	
		V_{GS}=-1.8V, I_{DS}=-1A	-	160	240	
gfs	Forward Transconductance	V_{DS}=-5V, I_{DS}=-1.5A	-	5	-	S
Dynamic Characteristics ⑤						
R_G	Gate Resistance	V_{GS}=0V,V_{DS}=0V, Freq.=1MHz	-	9	-	Ω
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-10V, Freq.=1MHz	-	304	-	pF
C_{oss}	Output Capacitance		-	37	-	
C_{rss}	Reverse Transfer Capacitance		-	33	-	
$td_{(ON)}$	Turn-on Delay Time	V_{GS}=-4.5V,V_{DS}=-10V, I_D=-1A,R_{GEN}=6Ω	-	1.2	-	nS
t_r	Turn-on Rise Time		-	24	-	
$t_{d(OFF)}$	Turn-off Delay Time		-	23	-	
t_f	Turn-off Fall Time		-	16	-	
Q_g	Total Gate Charge	V_{GS}=-2.5V,V_{DS}=-10V I_D=-1.5A	-	2.8	-	nC
Q_g	Total Gate Charge	V_{GS}=-4.5V,V_{DS}=-10V, I_D=-1.5A	-	4.9	-	
Q_{gs}	Gate-Source Charge		-	0.8	-	
Q_{gd}	Gate-Drain Charge		-	1.1	-	
Source-Drain Characteristics						
V_{SD}④	Diode Forward Voltage	I_{SD}=-2A, V_{GS}=0V	-	-0.9	-1.1	V
t_{rr}	Reverse Recovery Time	I_F=-3A, V_R=0 dI$_F$/dt=100A/μs	-	30	-	nS
Q_{rr}	Reverse Recovery Charge		-	4	-	nC

Note ④：Pulse test (pulse width≤300us, duty cycle≤2%).
Note ⑤：Guaranteed by design, not subject to production testing.

P-Channel Typical Characteristics

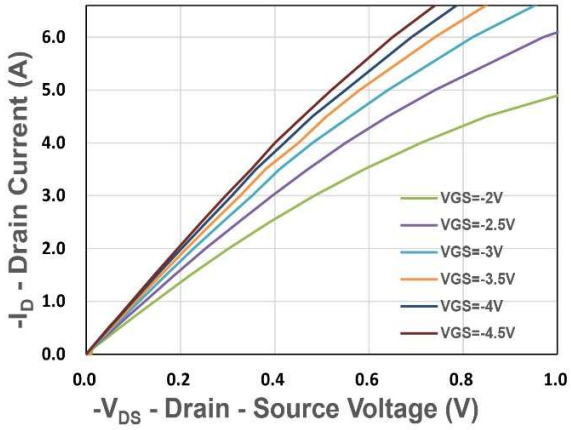


Figure 1. Output Characteristics

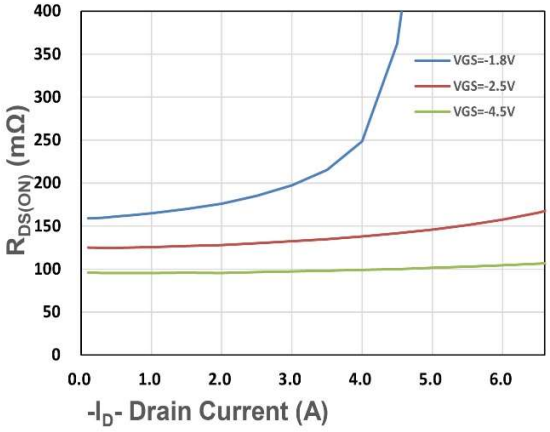


Figure 2. On-Resistance vs. ID

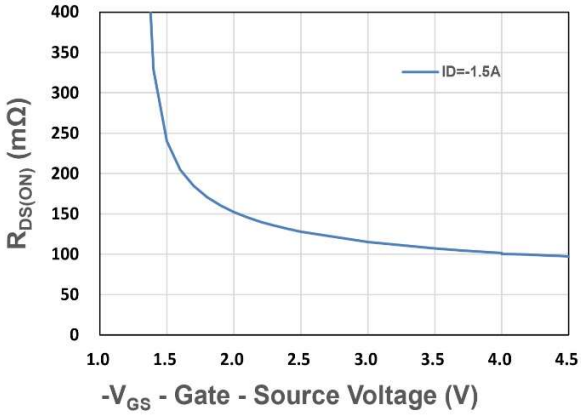


Figure 3. On-Resistance vs. VGS

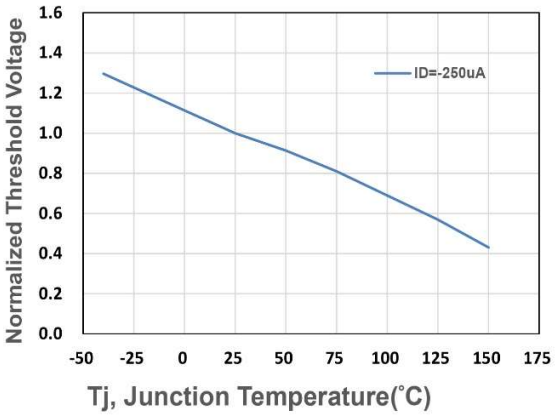


Figure 4. Gate Threshold Voltage

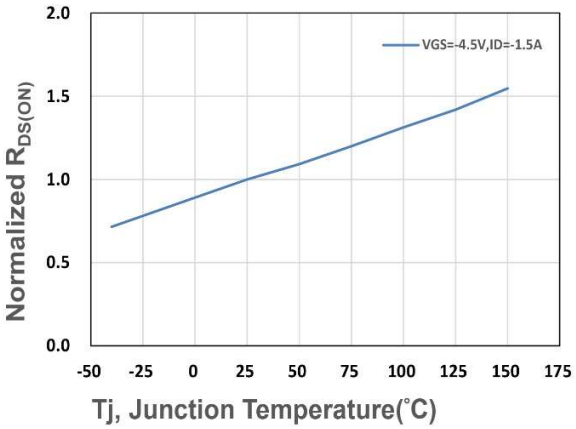


Figure 5. Drain-Source On Resistance

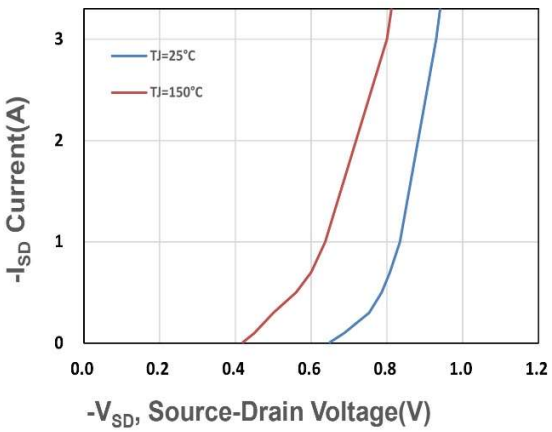


Figure 6. Source-Drain Diode Forward

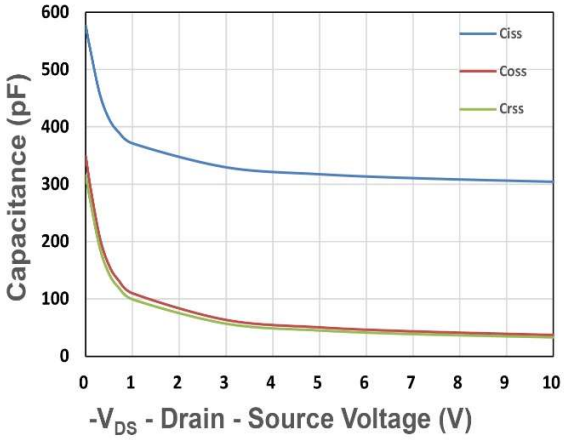


Figure 7. Capacitance

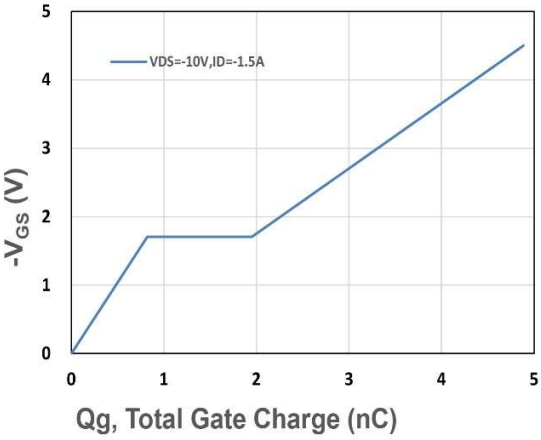


Figure 8. Gate Charge Characteristics

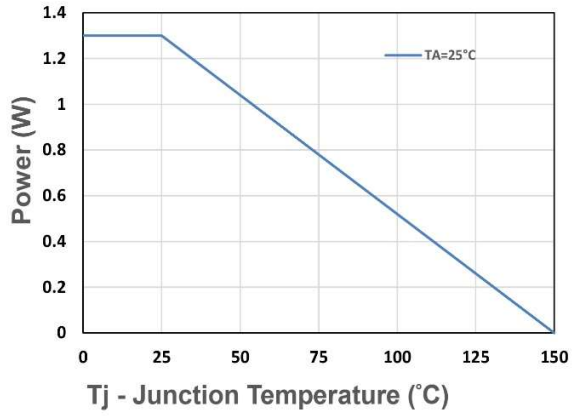


Figure 9. Power Dissipation

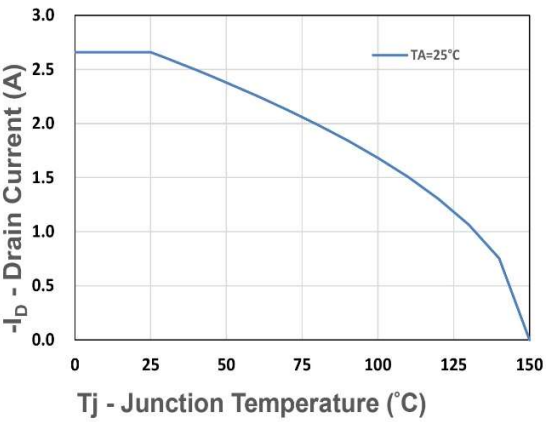


Figure 10. Drain Current

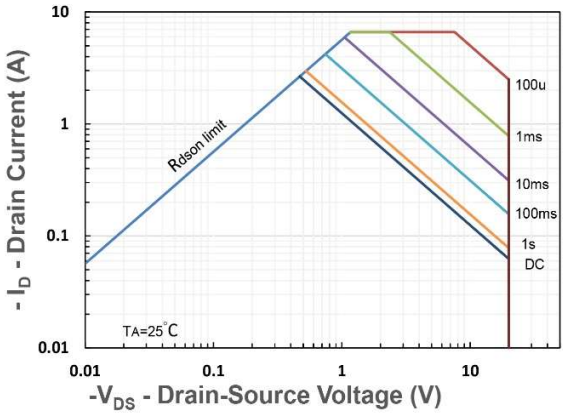


Figure 11. Safe Operating Area

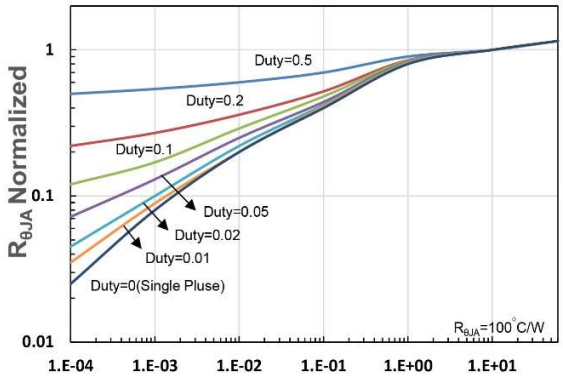


Figure 12. RθJA Transient Thermal Impedance