




# Power MOSFETS


## DATASHEET

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**LM30048NAK8A**

N-Channel  
Enhancement Mode MOSFET

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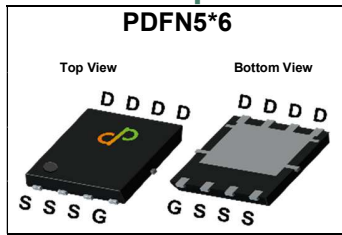


Quality Management Systems

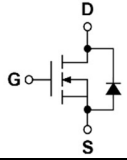
ISO 9001:2015 Certificate

## N-Channel Enhancement Mode MOSFET

### Pin Description



### Symbol



### Ordering Information

Symbol	N-Channel	Unit
$V_{DSS}$	30	V
$R_{DS(ON)-Max}$	4.8	m $\Omega$
$I_D$	70	A

### Feature

- Lower  $R_{DS(ON)}$  to Minimize Conduction Losses
- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- 100% UIS Tested

### Applications

- Power Management in Notebook Computer
- Battery Powered System

### Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM30048NAK8A	PDFN5*6	Tape & Reel	5000 / Tape & Reel	30048 □□□□□□

Note : □□□□□□ = Lot Code

### Absolute Maximum Ratings (T<sub>J</sub>=25°C Unless Otherwise Noted)

Symbol	Parameter	N-Channel	Unit	
$V_{DSS}$	Drain-Source Voltage	30	V	
$V_{GSS}$	Gate-Source Voltage	±20		
$T_J$	Maximum Junction Temperature	150	°C	
$T_{STG}$	Storage Temperature Range	-55 to 150	°C	
$I_{DM}^{①}$	Pulse Drain Current Tested	T <sub>c</sub> =25°C	70	A
$I_D$	Continuous Drain Current	T <sub>c</sub> =25°C	70	A
		T <sub>c</sub> =100°C	48	
$P_D$	Maximum Power Dissipation	T <sub>c</sub> =25°C	42	W
		T <sub>c</sub> =100°C	17	
$I_{AS}^{②}$	Avalanche Current, Single pulse	L=0.1mH	28	A
$E_{AS}^{②}$	Avalanche Energy, Single pulse	L=0.1mH	39	mJ

### Thermal Characteristics

Symbol	Parameter	Rating	Unit	
$R_{\theta JC}$	Thermal Resistance-Junction to Case	Steady State	3	°C/W
$R_{\theta JA}^{③}$	Thermal Resistance-Junction to Ambient	Steady State	50	°C/W

Note ① : Max. current is limited by bonding wire.

Note ② : UIS tested and pulse width are limited by maximum junction temperature 150°C

Note ③ : Surface Mounted on 1in<sup>2</sup> FR-4 board with 1 $\phi$

## N-Channel Electrical Characteristics (T<sub>J</sub>=25°C Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static Electrical Characteristics</b>						
<b>BV<sub>DSS</sub></b>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>DS</sub> =250uA	30	-	-	V
<b>I<sub>DSS</sub></b>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =24V, V <sub>GS</sub> =0V	-	-	1	uA
<b>V<sub>GS(th)</sub></b>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>DS</sub> =250uA	1.1	1.6	2.1	V
<b>I<sub>GSS</sub></b>	Gate Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
<b>R<sub>DS(ON)</sub></b> <sup>④</sup>	Drain-Source On-state Resistance	V <sub>GS</sub> =10V, I <sub>DS</sub> =20A	-	4.1	4.8	mΩ
		V <sub>GS</sub> =4.5V, I <sub>DS</sub> =18A	-	5.3	6.9	
<b>gfs</b>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>DS</sub> =20A	-	22	-	S
<b>Dynamic Characteristics</b> <sup>⑥</sup>						
<b>R<sub>G</sub></b>	Gate Resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, Freq.=1MHz	-	2.2	-	Ω
<b>C<sub>iss</sub></b>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, Freq.=1MHz	-	1860	-	pF
<b>C<sub>oss</sub></b>	Output Capacitance		-	260	-	
<b>C<sub>rss</sub></b>	Reverse Transfer Capacitance		-	212	-	
<b>td(ON)</b>	Turn-on Delay Time	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, I <sub>D</sub> =1A, R <sub>GEN</sub> =6Ω	-	9.6	-	nS
<b>t<sub>r</sub></b>	Turn-on Rise Time		-	23.4	-	
<b>t<sub>d(OFF)</sub></b>	Turn-off Delay Time		-	62.8	-	
<b>t<sub>f</sub></b>	Turn-off Fall Time		-	23	-	
<b>Q<sub>g</sub></b>	Total Gate Charge	V <sub>GS</sub> =4.5V, V <sub>DS</sub> =15V, I <sub>D</sub> =14A	-	26	-	nC
<b>Q<sub>g</sub></b>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, I <sub>D</sub> =14A	-	48	-	
<b>Q<sub>gs</sub></b>	Gate-Source Charge		-	3.4	-	
<b>Q<sub>gd</sub></b>	Gate-Drain Charge		-	14	-	
<b>Source-Drain Characteristics</b>						
<b>V<sub>SD</sub></b> <sup>④</sup>	Diode Forward Voltage	I <sub>SD</sub> =2A, V <sub>GS</sub> =0V	-	0.75	1.1	V
<b>t<sub>rr</sub></b>	Reverse Recovery Time	I <sub>F</sub> =2A, V <sub>R</sub> =15V	-	18.2	-	nS
<b>Q<sub>rr</sub></b>	Reverse Recovery Charge	dI <sub>F</sub> /dt=100A/μs	-	9.2	-	nC

Note ④ : Pulse test (pulse width≤300us, duty cycle≤2%).

Note ⑤ : Guaranteed by design, not subject to production testing.

## N-Channel Typical Characteristics

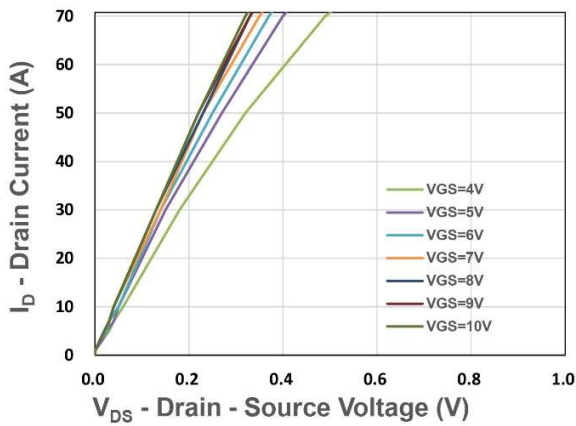


Figure 1. Output Characteristics

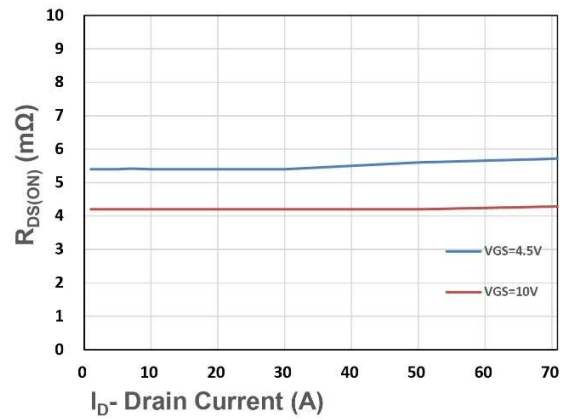


Figure 2. On-Resistance vs. ID

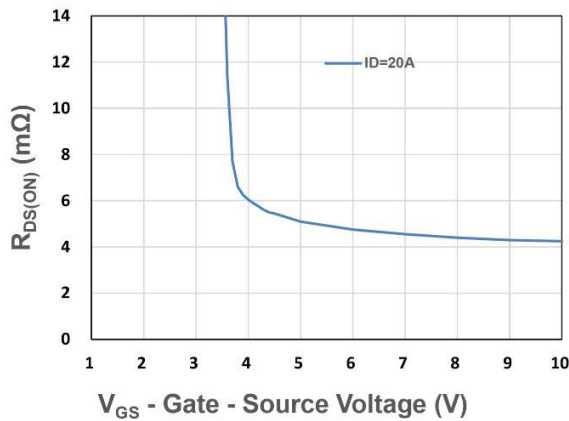


Figure 3. On-Resistance vs. VGS

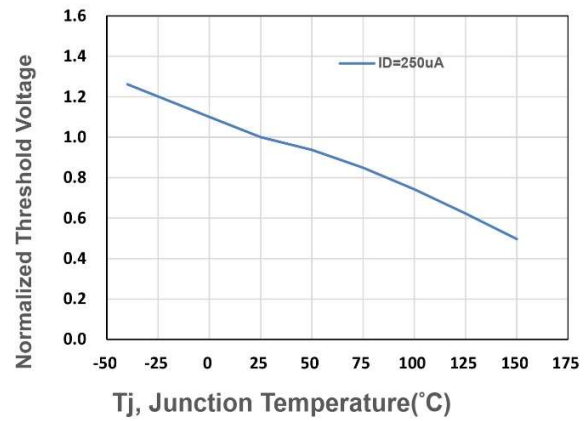


Figure 4. Gate Threshold Voltage

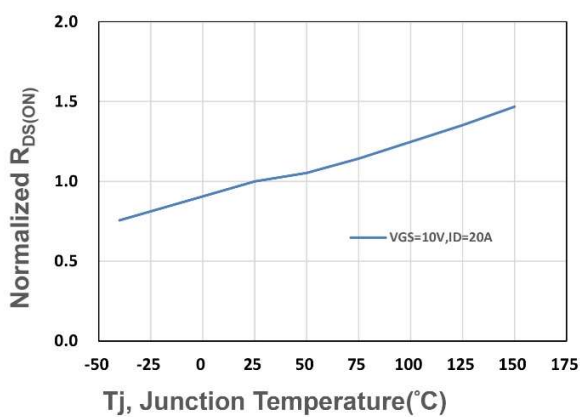


Figure 5. Drain-Source On Resistance

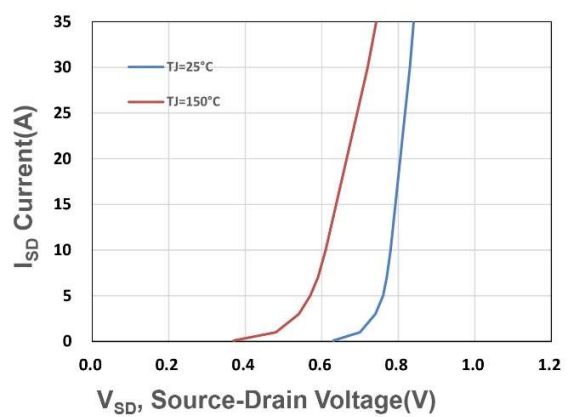
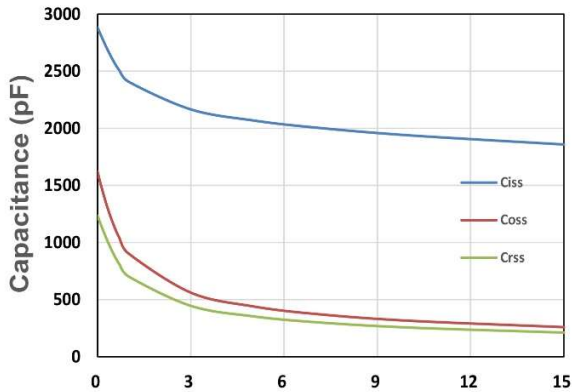
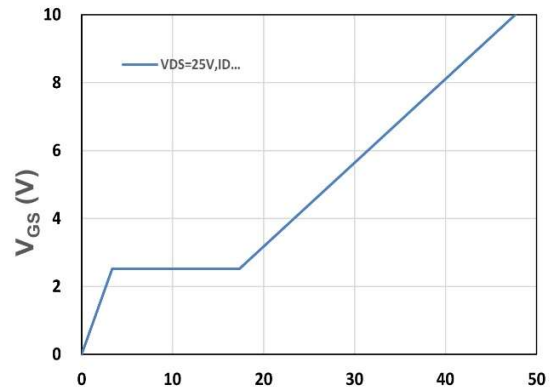


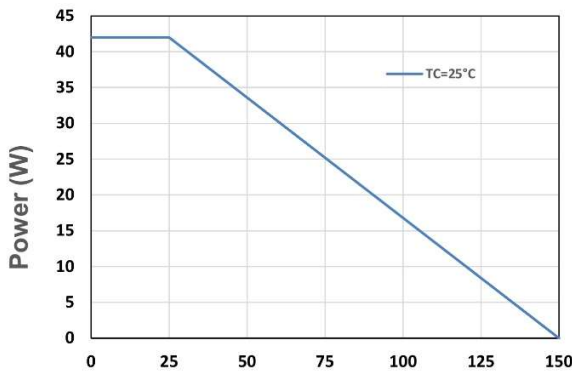
Figure 6. Source-Drain Diode Forward



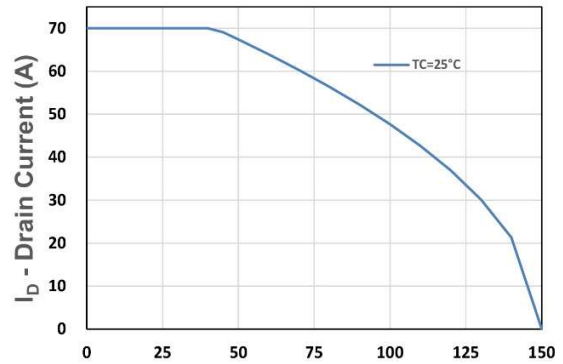
$V_{DS}$  - Drain - Source Voltage (V)  
Figure 7. Capacitance



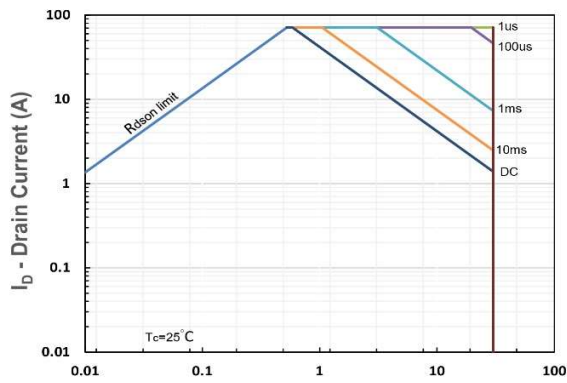
$Q_g$ , Total Gate Charge (nC)  
Figure 8. Gate Charge Characteristics



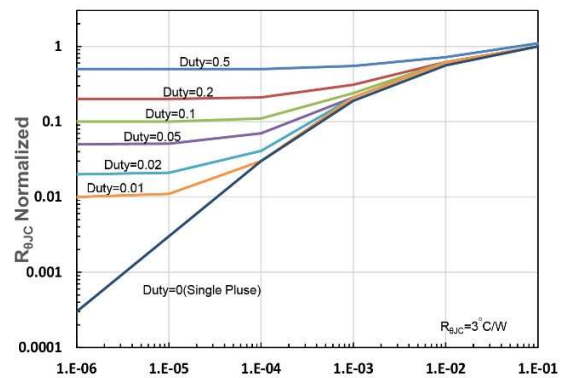
$T_j$  - Junction Temperature ( $^{\circ}C$ )  
Figure 9. Power Dissipation



$T_j$  - Junction Temperature ( $^{\circ}C$ )  
Figure 10. Drain Current



$V_{DS}$  - Drain- Source Voltage (V)  
Figure 11. Safe Operating Area



$t_1$ , Square Wave Pulse Duration(s)  
Figure 12.  $R_{\theta,jc}$  Transient Thermal Impedance