





Power MOSFETS


DATASHEET

LM30072PAK8A

P-Channel
Enhancement Mode MOSFET

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Quality Management Systems

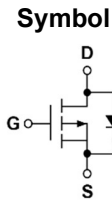
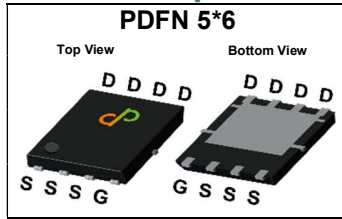
ISO 9001:2015 Certificate

LM30072PAK8A



P-Channel Enhancement Mode MOSFET

Pin Description



Ordering Information

Symbol	P-Channel	Unit
V_{DSS}	-30	V
$R_{DS(ON)-Max}$	8	m Ω
I_D	-67	A

Feature

- Low Rdson application
- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- 100% UIS Tested

Applications

- DC-DC converters
- Battery Powered System

Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM30072PAK8A	PDFN5*6	Tape & Reel	5000 / Tape & Reel	30072 □□□□□□

Note : □□□□□□ = Lot Code

Absolute Maximum Ratings (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter	P-Channel	Unit
V_{DSS}	Drain-Source Voltage	-30	V
V_{GSS}	Gate-Source Voltage	±20	
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-55 to 150	°C
$I_{DM}^{①}$	Pulse Drain Current Tested	T _c =25°C -141	A
I_D	Continuous Drain Current	T _c =25°C -67	A
		T _c =100°C -43	
P_D	Maximum Power Dissipation	T _c =25°C 50	W
		T _c =100°C 20	
$I_{AS}^{②}$	Avalanche Current, Single pulse	L=0.1mH -33	A
$E_{AS}^{②}$	Avalanche Energy, Single pulse	L=0.1mH 55	mJ

Thermal Characteristics

Symbol	Parameter	Rating	Unit
$R_{\theta JC}$	Thermal Resistance-Junction to Case	Steady State 2.5	°C/W
$R_{\theta JA}^{③}$	Thermal Resistance-Junction to Ambient	Steady State 50	°C/W

Note ① : Max. current is limited by bonding wire.

Note ② : UIS tested and pulse width are limited by maximum junction temperature 150°C.

Note ③ : Surface Mounted on 1in² FR-4 board with 1oz.

P-Channel Electrical Characteristics (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Electrical Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =-250uA	-30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-24V, V _{GS} =0V	-	-	-1	uA
V_{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =-250uA	-1	-1.5	-2	V
I_{GSS}	Gate Leakage Current	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
R_{DS(ON)} ^④	Drain-Source On-state Resistance	V _{GS} =-10V, I _{DS} =-12A	-	6.5	8	mΩ
		V _{GS} =-4.5V, I _{DS} =-9A	-	8.2	10.7	
gfs	Forward Transconductance	V _{DS} =-5V, I _{DS} =-12A	-	35	-	S
Dynamic Characteristics ^⑤						
R_G	Gate Resistance	V _{GS} =0V, V _{DS} =0V, Freq.=1MHz	-	11	-	Ω
C_{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-15V, Freq.=1MHz	-	4430	-	pF
C_{oss}	Output Capacitance					
C_{rss}	Reverse Transfer Capacitance					
td(ON)	Turn-on Delay Time	V _{GS} =-10V, V _{DS} =-15V, I _D =-1A, R _{GEN} =3Ω	-	51	-	nS
t_r	Turn-on Rise Time					
t_{d(OFF)}	Turn-off Delay Time					
t_f	Turn-off Fall Time					
Q_g	Total Gate Charge	V _{GS} =-4.5V, V _{DS} =-15V, I _D =-10A	-	42	-	nC
Q_g	Total Gate Charge	V _{GS} =-10V, V _{DS} =-15V, I _D =-10A	-	88	-	
Q_{gs}	Gate-Source Charge		-	14	-	
Q_{gd}	Gate-Drain Charge		-	8.5	-	
Source-Drain Characteristics						
V_{SD} ^④	Diode Forward Voltage	I _{SD} =-3.6A, V _{GS} =0V	-	-0.75	-1.1	V
t_{rr}	Reverse Recovery Time	I _F =-3.6A, V _R =-10V	-	25	-	nS
Q_{rr}	Reverse Recovery Charge	dI _F /dt=100A/μs	-	15	-	nC

Note ④ : Pulse test (pulse width≤300us, duty cycle≤2%).

Note ⑤ : Guaranteed by design, not subject to production testing.

P-Channel Typical Characteristics

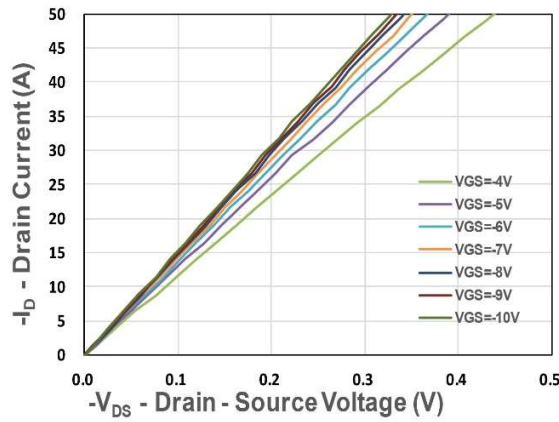


Figure 1. Output Characteristics

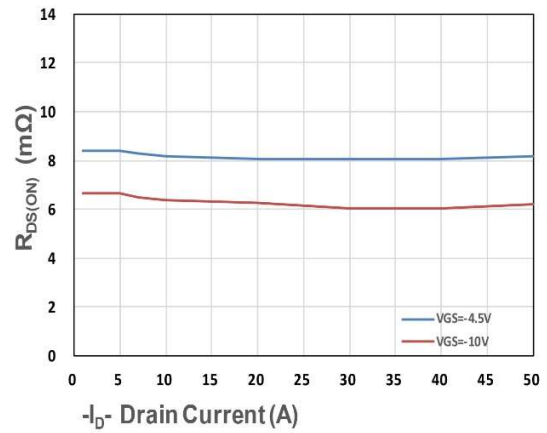


Figure 2. On-Resistance vs. ID

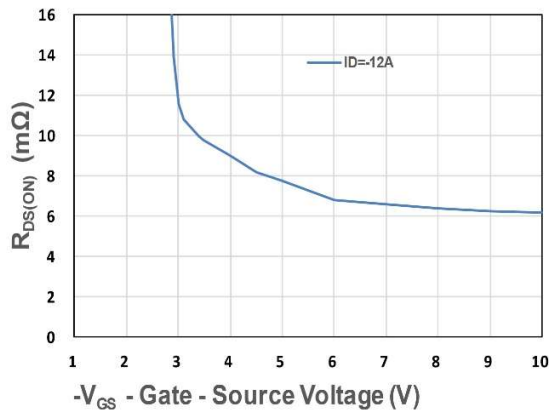


Figure 3. On-Resistance vs. V_GS

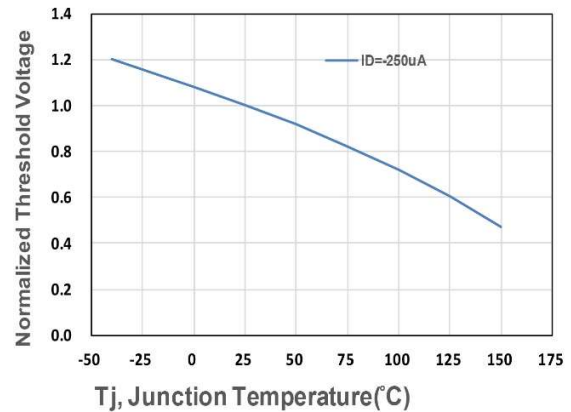


Figure 4. Gate Threshold Voltage

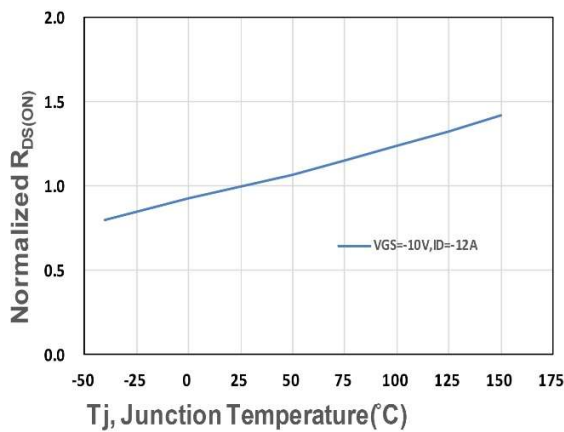


Figure 5. Drain-Source On Resistance

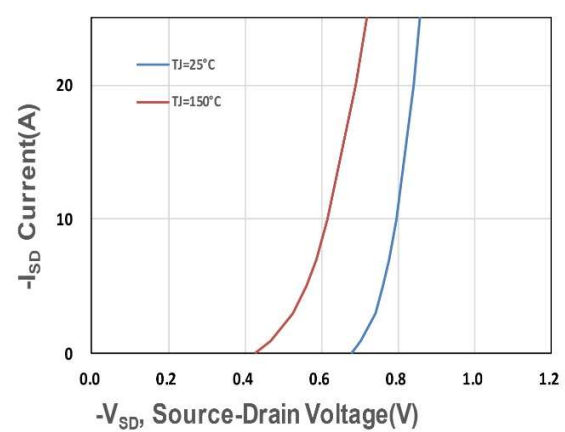


Figure 6. Source-Drain Diode Forward

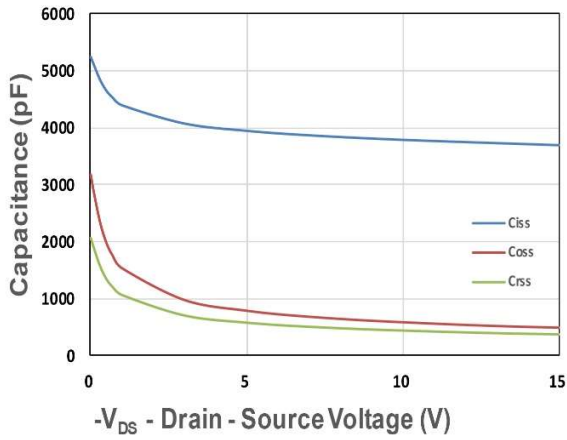


Figure 7. Capacitance

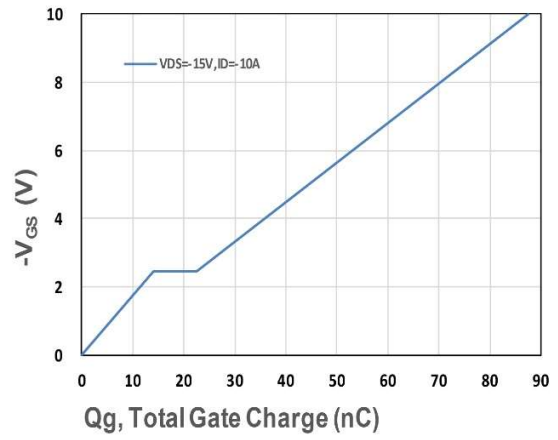


Figure 8. Gate Charge Characteristics

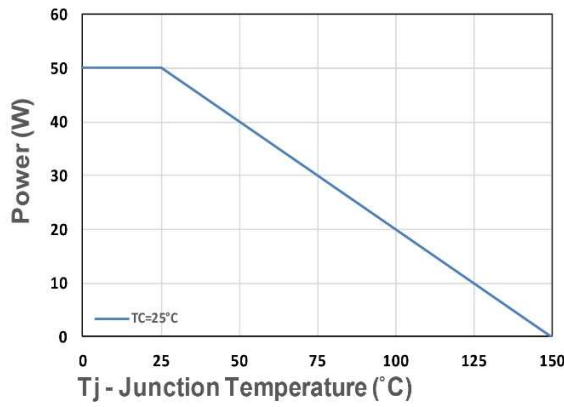


Figure 9. Power Dissipation

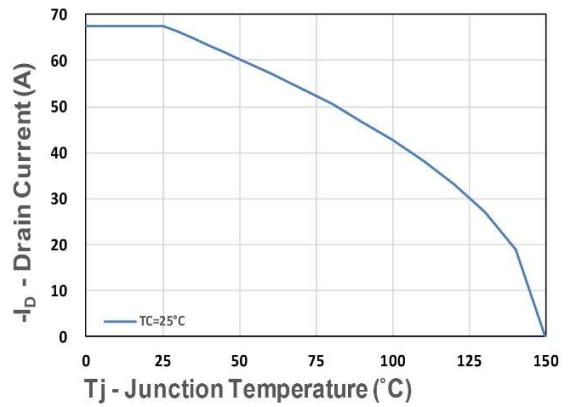


Figure 10. Drain Current

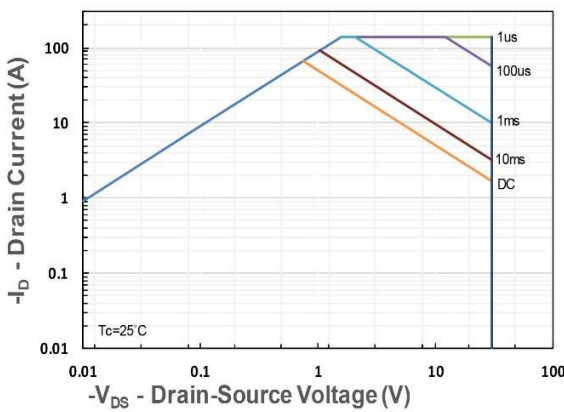


Figure 11. Safe Operating Area

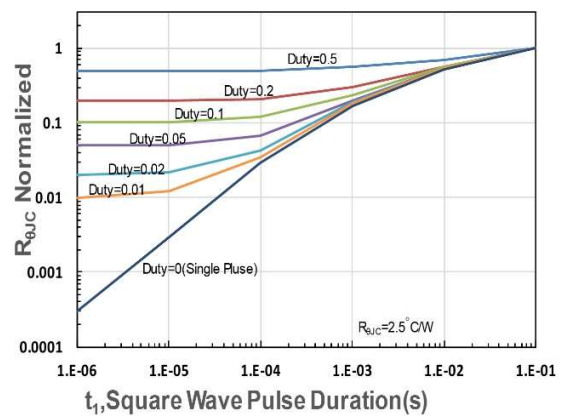


Figure 12. $R_{\theta JC}$ Transient Thermal Impedance