



Power MOSFETS

DATASHEET

LM30160TAQ8A

Dual P-Channel
Enhancement Mode MOSFET

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Quality Management Systems

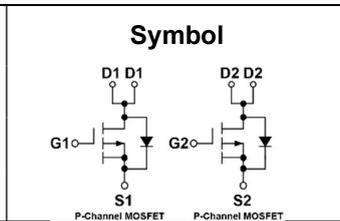
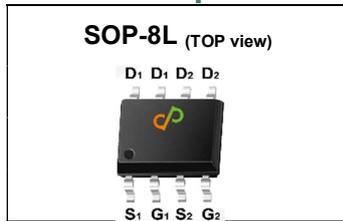
ISO 9001:2015 Certificate

LM30160TAQ8A



Dual P-Channel Enhancement Mode MOSFET

Pin Description



Ordering Information

Symbol	Dual P-Channel	Unit
V_{DSS}	-30	V
$R_{DS(ON)-Max}$	18	m Ω
I_D	-7.3	A

Feature

- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- Lower Qg and Qgd for high-speed switching
- Lower RDS(ON) to Minimize Conduction Losses
- 100% UIS Tested

Applications

- Power Management in DC/DC
- Power Load Switch

Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM30160TAQ8A	SOP-8L(Dual)	Tape & Reel	3000 / Tape & Reel	30160 □□□□□□

Note : □□□□□□ = Lot Code

Absolute Maximum Ratings (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter	Dual P-Channel	Unit
V_{DSS}	Drain-Source Voltage	-30	V
V_{GSS}	Gate-Source Voltage	±25	
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-55 to 150	°C
$I_{DM}^{①}$	Pulse Drain Current Tested	$T_A=25^\circ\text{C}$ -18	A
$I_D^{②}$	Continuous Drain Current	$T_A=25^\circ\text{C}$ -7.3	A
		$T_A=70^\circ\text{C}$ -5.8	
$P_D^{③}$	Maximum Power Dissipation	$T_A=25^\circ\text{C}$ 1.5	W
		$T_A=70^\circ\text{C}$ 0.9	
$I_{AS}^{③}$	Avalanche Current, Single pulse	L=0.1mH -18	A
$E_{AS}^{②}$	Avalanche Energy, Single pulse	L=0.1mH 16	mJ

Thermal Characteristics

Symbol	Parameter	Rating	Unit
$R_{\theta JA}^{③}$	Thermal Resistance-Junction to Ambient	t<=10s 44	°C/W
		Steady State 85	°C/W

Note ① : Max. current is limited by junction temperature.

Note ② : UIS tested and pulse width are limited by maximum junction temperature 150°C

Note ③ : Surface Mounted on 1in² FR-4 board with 1oz.

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Dual P-Channel Electrical Characteristics (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Electrical Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =-250uA	-30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-24V, V _{GS} =0V	-	-	-1	uA
V_{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =-250uA	-1	-1.5	-2	V
I_{GSS}	Gate Leakage Current	V _{GS} =±25V, V _{DS} =0V	-	-	±100	nA
R_{DS(ON)}^④	Drain-Source On-state Resistance	V _{GS} =-10V, I _{DS} =-10A	-	15	18	mΩ
		V _{GS} =-4.5V, I _{DS} =-7A	-	18	23	
gfs	Forward Transconductance	V _{DS} =-10V, I _{DS} =-5A	-	14.7	-	S
Dynamic Characteristics^⑤						
R_G	Gate Resistance	V _{GS} =0V, V _{DS} =0V, Freq.=1MHz	-	8.9	-	Ω
C_{ISS}	Input Capacitance	V _{GS} =0V, V _{DS} =-15V, Freq.=1MHz	-	2157	-	pF
C_{OSS}	Output Capacitance					
C_{RSS}	Reverse Transfer Capacitance					
td(ON)	Turn-on Delay Time	V _{GS} =-10V, V _{DS} =-15V, I _D =-1A, R _{GEN} =6Ω	-	10.6	-	nS
t_r	Turn-on Rise Time					
t_{d(OFF)}	Turn-off Delay Time					
t_f	Turn-off Fall Time					
Q_g	Total Gate Charge	V _{GS} =-4.5V, V _{DS} =-15V, I _D =-10A	-	23	-	nC
Q_g	Total Gate Charge	V _{GS} =-10V, V _{DS} =-15V, I _D =-10A	-	46	-	
Q_{gs}	Gate-Source Charge		-	6.5	-	
Q_{gd}	Gate-Drain Charge		-	8.8	-	
Source-Drain Characteristics						
V_{SD}^④	Diode Forward Voltage	I _{SD} =-5A, V _{GS} =0V	-	-0.75	-1.1	V
t_{rr}	Reverse Recovery Time	I _F =-5A, V _R =-15V,	-	13.4	-	nS
Q_{rr}	Reverse Recovery Charge	dI _F /dt=1A/μs	-	7.1	-	nC

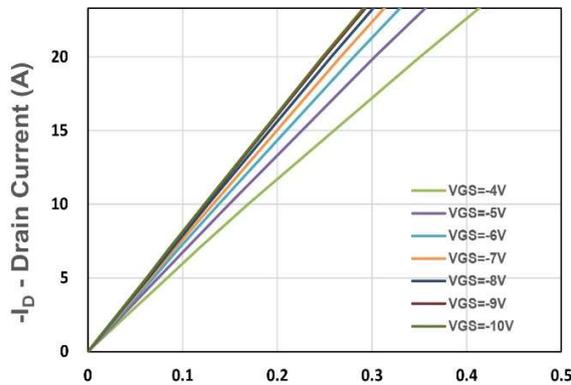
Note ④ : Pulse test (pulse width≤300us, duty cycle≤2%).

Note ⑤ : Guaranteed by design, not subject to production testing.

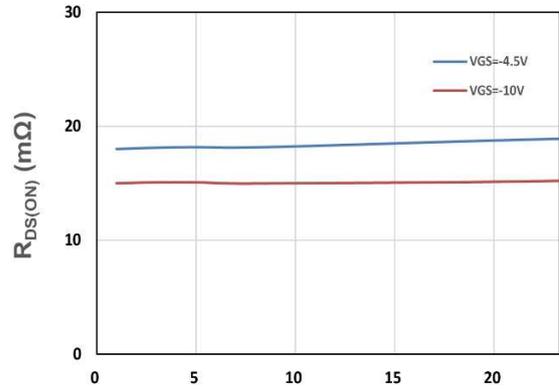
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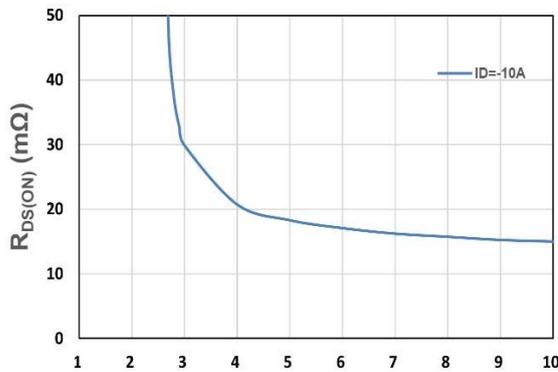
Dual P-Channel Typical Characteristics



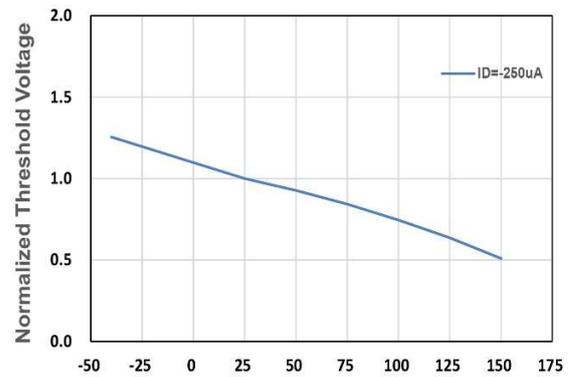
$-V_{DS}$ - Drain - Source Voltage (V)
Figure 1. Output Characteristics



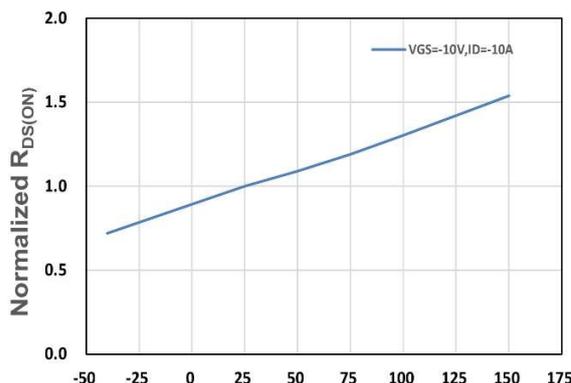
$-I_D$ - Drain Current (A)
Figure 2. On-Resistance vs. ID



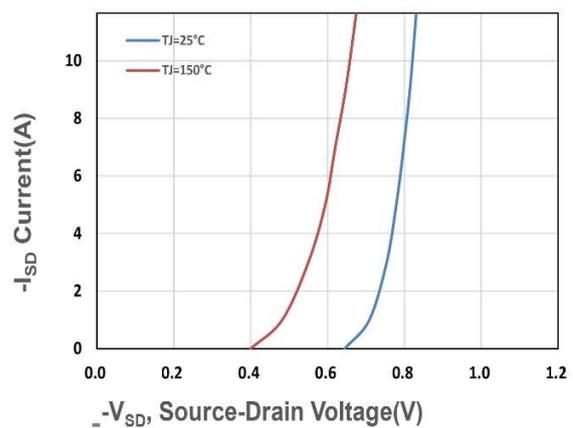
$-V_{GS}$ - Gate - Source Voltage (V)
Figure 3. On-Resistance vs. VGS



T_j , Junction Temperature (°C)
Figure 4. Gate Threshold Voltage

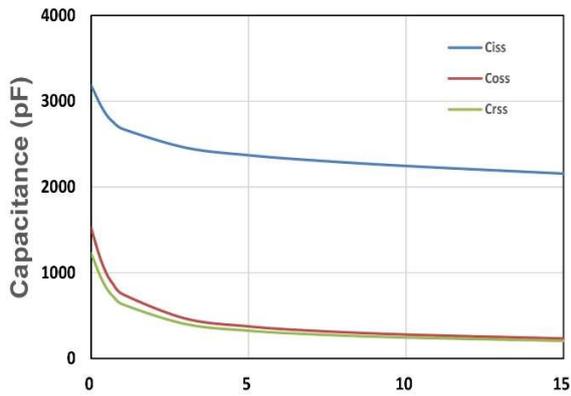


T_j , Junction Temperature (°C)
Figure 5. Drain-Source On Resistance

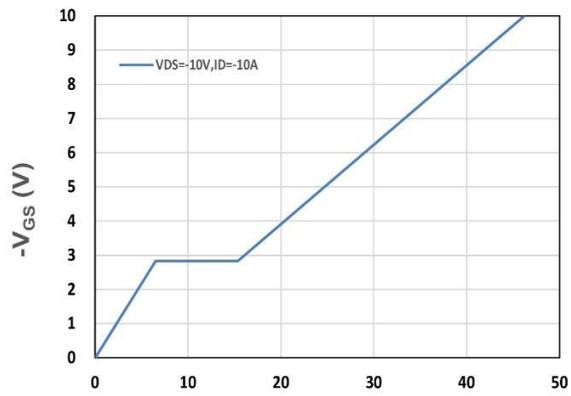


$-V_{SD}$, Source-Drain Voltage (V)
Figure 6. Source-Drain Diode Forward

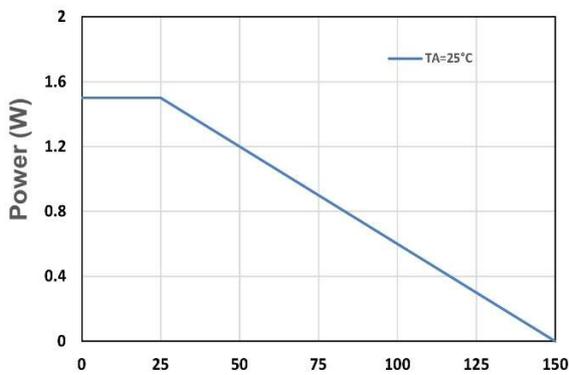
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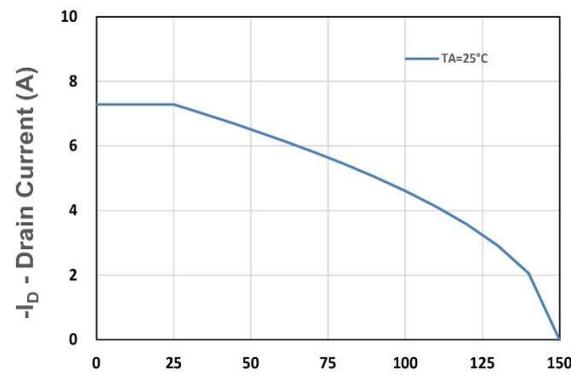
$-V_{DS}$ - Drain - Source Voltage (V)
Figure 7. Capacitance



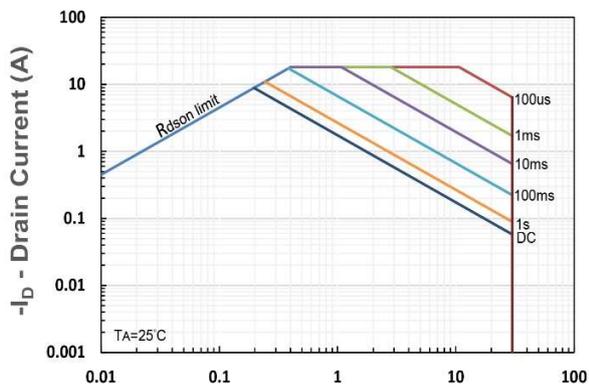
Qg , Total Gate Charge (nC)
Figure 8. Gate Charge Characteristics



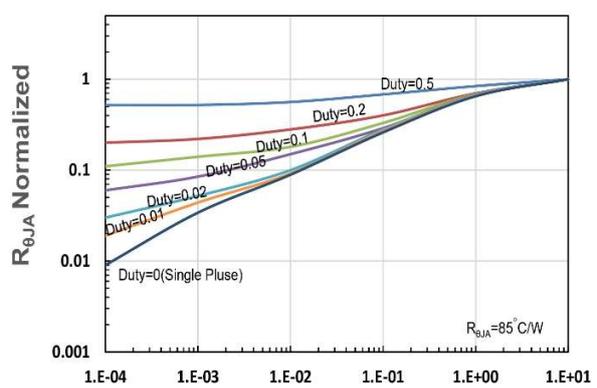
Tj - Junction Temperature (°C)
Figure 9. Power Dissipation



Tj - Junction Temperature (°C)
Figure 10. Drain Current



V_{DS} - Drain-Source Voltage (V)
Figure 11. Safe Operating Area



t_1 , Square Wave Pulse Duration (s)
Figure 12. $R_{\theta JA}$ Transient Thermal Impedance