




# Power MOSFETS


## DATASHEET


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**LM30440PLI3A**

P-Channel  
Enhancement Mode MOSFET

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Quality Management Systems

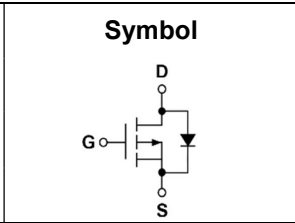
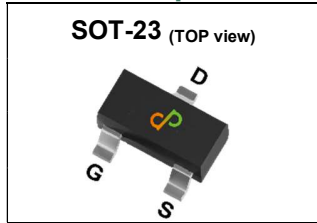
ISO 9001:2015 Certificate

# LM30440PLI3A



## P-Channel Enhancement Mode MOSFET

### Pin Description



### Product Summary

Symbol	P-Channel	Unit
V <sub>DSS</sub>	-30	V
R <sub>DS(ON)-Max</sub>	48	mΩ
I <sub>D</sub>	-4.2	A

### Feature

- Low input Capacitance
- Reliable and Rugged
- ROHS Compliant & Halogen-Free

### Applications

- Motor control
- Backlighting
- DC-DC Converters

### Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM30440PLI3A	SOT-23	Tape & Reel	3000 / Tape & Reel	03□□□

Note : □□□ = Lot Code

### Absolute Maximum Ratings (T<sub>J</sub>=25°C Unless Otherwise Noted)

Symbol	Parameter	P-Channel	Unit	
V <sub>DSS</sub>	Drain-Source Voltage	-30	V	
V <sub>GSS</sub>	Gate-Source Voltage	±12		
T <sub>J</sub>	Maximum Junction Temperature	150	°C	
T <sub>STG</sub>	Storage Temperature Range	-55 to 150	°C	
I <sub>DM</sub> <sup>①</sup>	Pulse Drain Current Tested	T <sub>A</sub> =25°C	-10.5	A
I <sub>D</sub>	Continuous Drain Current	T <sub>A</sub> =25°C	-4.2	A
		T <sub>A</sub> =70°C	-3.4	
P <sub>D</sub>	Maximum Power Dissipation	T <sub>A</sub> =25°C	1.1	W
		T <sub>A</sub> =70°C	0.73	

### Thermal Characteristics

Symbol	Parameter	Rating	Unit	
R <sub>θJA</sub> <sup>②</sup>	Thermal Resistance-Junction to Ambient	Steady State	110	°C/W

Note ① : Max. current is limited by junction temperature.

Note ② : Surface Mounted on 1in<sup>2</sup> FR-4 board with 1oz.

## P-Channel Electrical Characteristics (T<sub>J</sub>=25°C Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static Electrical Characteristics</b>						
<b>BV<sub>DSS</sub></b>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>DS</sub> =-250uA	-30	-	-	V
<b>I<sub>DSS</sub></b>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-24V, V <sub>GS</sub> =0V	-	-	-1	uA
<b>V<sub>GS(th)</sub></b>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>DS</sub> =-250uA	-0.5	-0.75	-1	V
<b>I<sub>GSS</sub></b>	Gate Leakage Current	V <sub>GS</sub> =±12V, V <sub>DS</sub> =0V	-	-	±100	nA
<b>R<sub>DS(on)</sub></b> <sup>③</sup>	Drain-Source On-state Resistance	V <sub>GS</sub> =-10V, I <sub>DS</sub> =-4A	-	40	48	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>DS</sub> =-3.7A	-	47	62	
		V <sub>GS</sub> =-2.5V, I <sub>DS</sub> =-2A	-	60	84	
<b>gfs</b>	Forward Transconductance	V <sub>DS</sub> =-5V, I <sub>DS</sub> =-4A	-	10	-	S
<b>Dynamic Characteristics</b> <sup>④</sup>						
<b>R<sub>G</sub></b>	Gate Resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, Freq.=1MHz	-	15.8	-	Ω
<b>C<sub>iss</sub></b>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =-15V, Freq.=1MHz	-	859	-	pF
<b>C<sub>oss</sub></b>	Output Capacitance		-	68	-	
<b>C<sub>rss</sub></b>	Reverse Transfer Capacitance		-	59	-	
<b>td(on)</b>	Turn-on Delay Time	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-15V, I <sub>D</sub> =-1A, R <sub>GEN</sub> =6Ω	-	8	-	nS
<b>t<sub>r</sub></b>	Turn-on Rise Time		-	13	-	
<b>t<sub>d(off)</sub></b>	Turn-off Delay Time		-	71	-	
<b>t<sub>f</sub></b>	Turn-off Fall Time		-	38	-	
<b>Q<sub>g</sub></b>	Total Gate Charge	V <sub>GS</sub> =-4.5V, V <sub>DS</sub> =-25V I <sub>D</sub> =-4A	-	11	-	nC
<b>Q<sub>g</sub></b>	Total Gate Charge	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-25V, I <sub>D</sub> =-4A	-	24	-	
<b>Q<sub>gs</sub></b>	Gate-Source Charge		-	2.4	-	
<b>Q<sub>gd</sub></b>	Gate-Drain Charge		-	3.5	-	
<b>Source-Drain Characteristics</b>						
<b>V<sub>SD</sub></b> <sup>④</sup>	Diode Forward Voltage	I <sub>SD</sub> =-1A, V <sub>GS</sub> =0V	-	-0.7	-1.1	V
<b>t<sub>rr</sub></b>	Reverse Recovery Time	I <sub>F</sub> =-1A, V <sub>R</sub> =-20V	-	39	-	nS
<b>Q<sub>rr</sub></b>	Reverse Recovery Charge	di <sub>F</sub> /dt=100A/μs	-	21	-	nC

Note ③ : Pulse test (pulse width≤300us, duty cycle≤2%).

Note ④ : Guaranteed by design, not subject to production testing.

## P-Channel Typical Characteristics

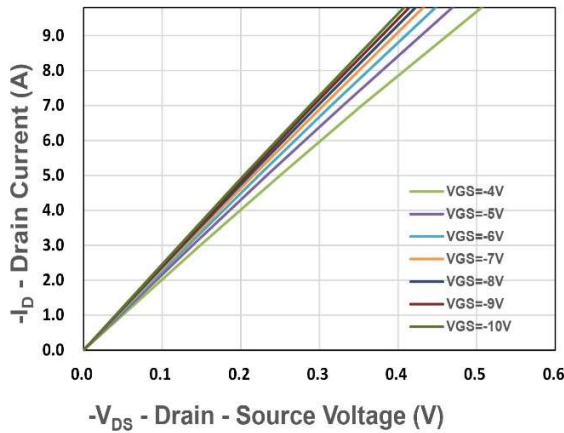


Figure 1. Output Characteristics

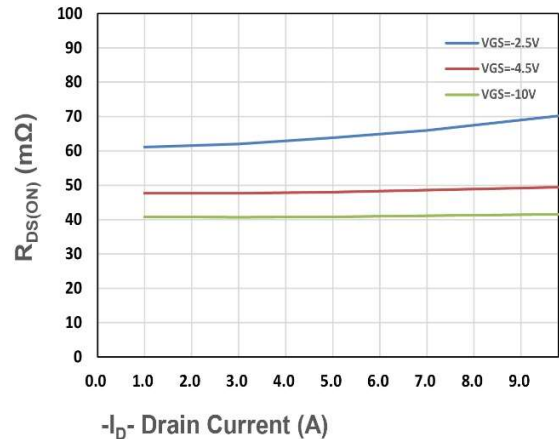


Figure 2. On-Resistance vs. ID

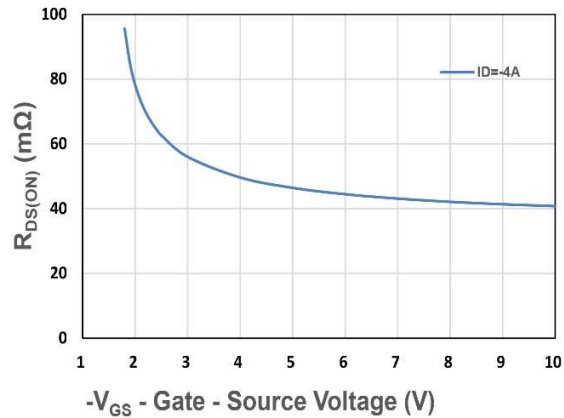


Figure 3. On-Resistance vs. VGS

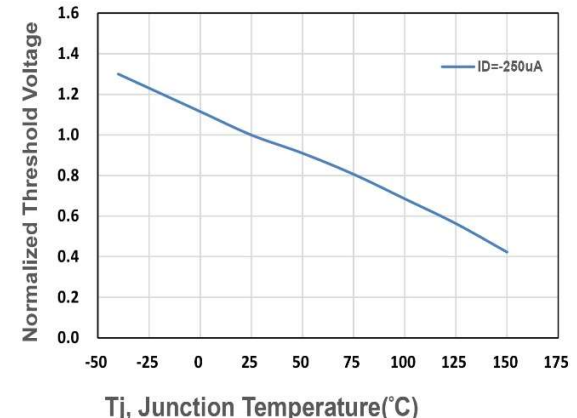


Figure 4. Gate Threshold Voltage

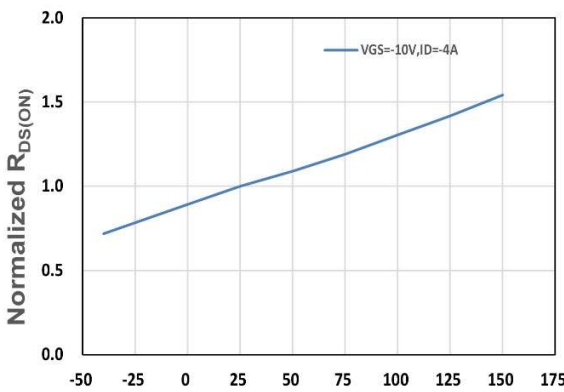


Figure 5. Drain-Source On Resistance

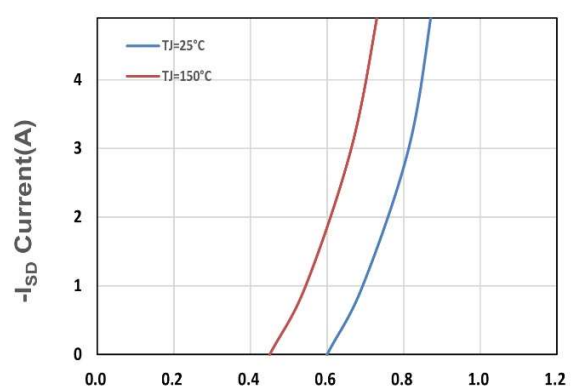
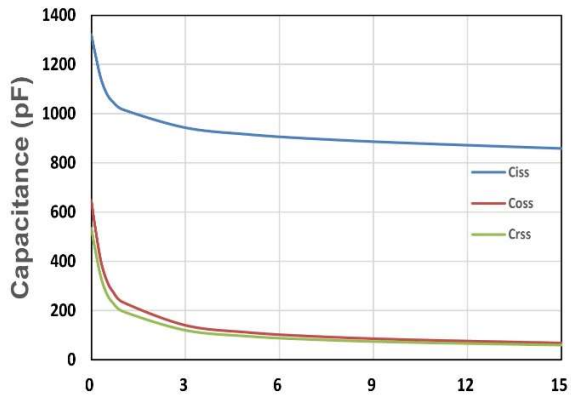
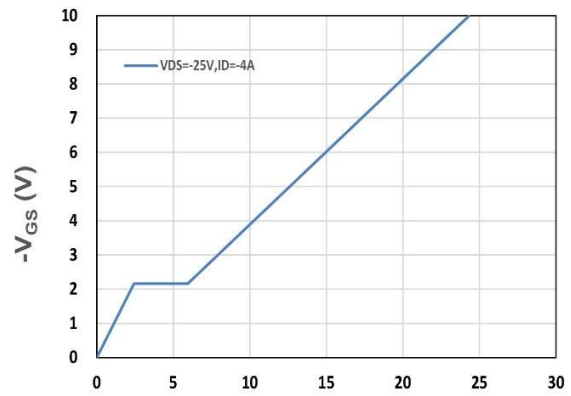


Figure 6. Source-Drain Diode Forward

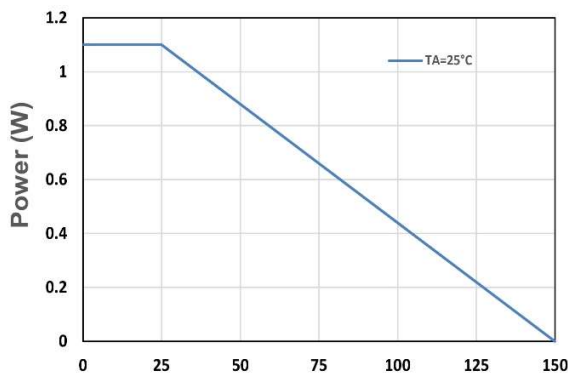
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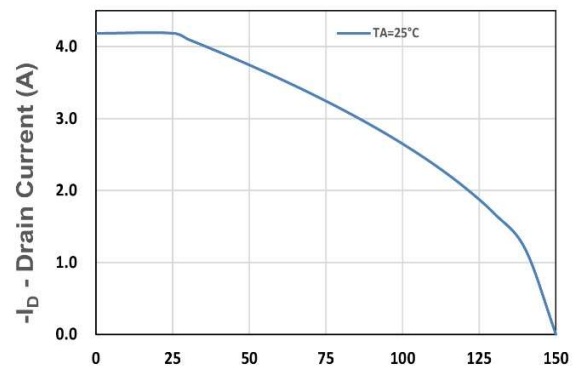
$-V_{DS}$  - Drain - Source Voltage (V)  
Figure 7. Capacitance



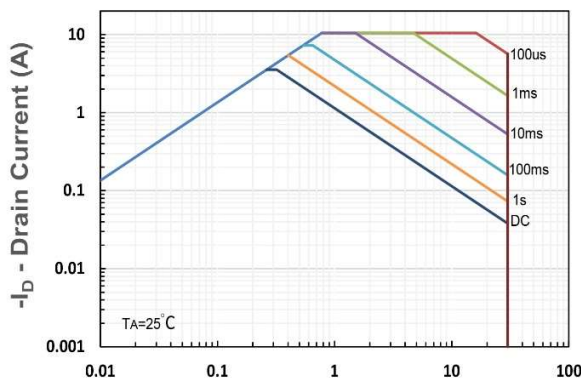
$Q_g$ , Total Gate Charge (nC)  
Figure 8. Gate Charge Characteristics



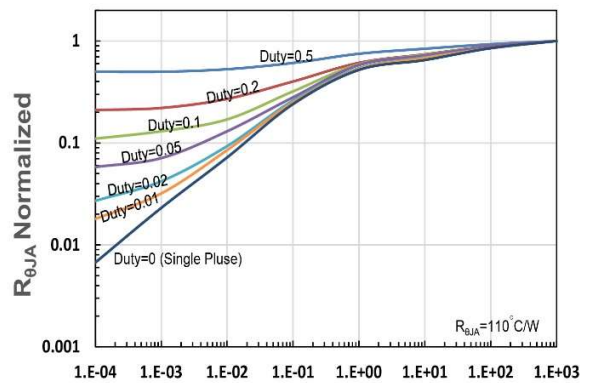
$T_j$  - Junction Temperature (°C)  
Figure 9. Power Dissipation



$T_j$  - Junction Temperature (°C)  
Figure 10. Drain Current



$-V_{DS}$  - Drain-Source Voltage (V)  
Figure 11. Safe Operating Area



$t_1$ , Square Wave Pulse Duration (s)  
Figure 12.  $R_{\theta JA}$  Transient Thermal Impedance