





Power MOSFETS


DATASHEET

LM30480TAQ8A

Dual P-Channel
Enhancement Mode MOSFET

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Quality Management Systems

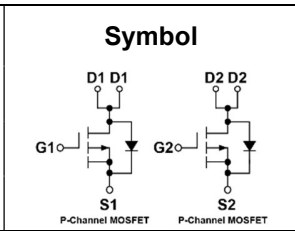
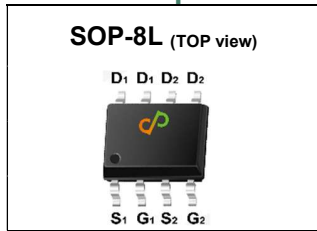
ISO 9001:2015 Certificate

LM30480TAQ8A



Dual P-Channel Enhancement Mode MOSFET

Pin Description



Product Summary

| Symbol | Dual P-Channel | Unit |
|------------------|----------------|------------|
| V_{DSS} | -30 | V |
| $R_{DS(ON)-Max}$ | 48 | m Ω |
| I_D | -3.5 | A |

Feature

- Fast switching speed
- Surface mount package
- Reliable and Rugged
- ROHS Compliant & Halogen-Free

Applications

- Load switch or in PWM applications

Ordering Information

| Orderable Part Number | Package Type | Form | Shipping | Marking |
|-----------------------|--------------|-------------|--------------------|-----------------|
| LM30480TAQ8A | SOP-8L | Tape & Reel | 3000 / Tape & Reel | 30480 □□□□□□ |

Note : □□□□□□ = Lot Code

Absolute Maximum Ratings (T_J=25°C Unless Otherwise Noted)

| Symbol | Parameter | | Dual P-Channel | Unit |
|--------------|----------------------------------|----------------------|----------------|------|
| V_{DSS} | Drain-Source Voltage | | -30 | V |
| V_{GSS} | Gate-Source Voltage | | ±20 | |
| T_J | Maximum Junction Temperature | | 150 | °C |
| T_{STG} | Storage Temperature Range | | -55 to 150 | °C |
| I_S | Diode Continuous Forward Current | T _A =25°C | -1 | A |
| $I_{DM}^{①}$ | Pulse Drain Current Tested | T _A =25°C | -8.7 | A |
| I_D | Continuous Drain Current | T _A =25°C | -3.5 | A |
| | | T _A =70°C | -2.8 | |
| P_D | Maximum Power Dissipation | T _A =25°C | 1.25 | W |
| | | T _A =70°C | 0.8 | |
| $I_{AS}^{②}$ | Avalanche Current, Single pulse | L=0.5mH | -6.8 | A |
| $E_{AS}^{②}$ | Avalanche Energy, Single pulse | L=0.5mH | 11 | mJ |

Thermal Characteristics

| Symbol | Parameter | | Rating | Unit |
|---------------------|--|--------------|--------|------|
| $R_{\theta JA}^{③}$ | Thermal Resistance-Junction to Ambient | t ≤ 10s | 78 | °C/W |
| | | Steady State | 100 | |

Note ① : Max. current is limited by junction temperature

Note ② : UIS tested and pulse width are limited by maximum junction temperature 150°C

Note ③ : Surface Mounted on 1in² FR-4 board with 1oz.

Dual P-Channel Electrical Characteristics (T_J=25°C Unless Otherwise Noted)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|----------------------------------|---|------|-------|------|------|
| Static Electrical Characteristics | | | | | | |
| BV_{DSS} | Drain-Source Breakdown Voltage | V _{GS} =0V, I _{DS} =-250uA | -30 | - | - | V |
| I_{DSS} | Zero Gate Voltage Drain Current | V _{DS} =-24V, V _{GS} =0V | - | - | -1 | uA |
| V_{GS(th)} | Gate Threshold Voltage | V _{DS} =V _{GS} , I _{DS} =-250uA | -0.8 | - | -2 | V |
| I_{GSS} | Gate Leakage Current | V _{GS} =±20V, V _{DS} =0V | - | - | ±100 | nA |
| R_{DS(ON)} ^④ | Drain-Source On-state Resistance | V _{GS} =-10V, I _{DS} =-5.2A | - | 40 | 48 | mΩ |
| | | V _{GS} =-4.5V, I _{DS} =-4A | - | 54 | 71 | |
| gfs | Forward Transconductance | V _{DS} =-10V, I _{DS} =-1A | - | 3.7 | - | S |
| Dynamic Characteristics ^⑤ | | | | | | |
| R_G | Gate Resistance | V _{GS} =0V, V _{DS} =0V, Freq.=1MHz | - | 28 | - | Ω |
| C_{iss} | Input Capacitance | V _{GS} =0V, V _{DS} =-15V, Freq.=1MHz | - | 619 | - | pF |
| C_{oss} | Output Capacitance | | | | | |
| C_{rss} | Reverse Transfer Capacitance | | | | | |
| td(ON) | Turn-on Delay Time | V _{GS} =-10V, V _{DS} =-15V, I _D =-1A, R _{GEN} =6Ω | - | 6 | - | nS |
| t_r | Turn-on Rise Time | | | | | |
| t_{d(OFF)} | Turn-off Delay Time | | | | | |
| t_f | Turn-off Fall Time | | | | | |
| Q_g | Total Gate Charge | V _{GS} =-4.5V, V _{DS} =-15V, I _D =-6A | - | 5.9 | - | nC |
| Q_g | Total Gate Charge | V _{GS} =-10V, V _{DS} =-15V, I _D =-6A | - | 13.1 | - | |
| Q_{gs} | Gate-Source Charge | | - | 1.6 | - | |
| Q_{gd} | Gate-Drain Charge | | - | 2.6 | - | |
| Source-Drain Characteristics | | | | | | |
| V_{SD} ^④ | Diode Forward Voltage | I _{SD} =-1.7A, V _{GS} =0V | - | -0.78 | -1.2 | V |
| t_{rr} | Reverse Recovery Time | I _F =-4.5A, V _R =0V | - | 8 | - | nS |
| Q_{rr} | Reverse Recovery Charge | dI _F /dt=100A/μs | - | 3 | - | nC |

Note ④ : Pulse test (pulse width≤300us, duty cycle≤2%).

Note ⑤ : Guaranteed by design, not subject to production testing.

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Dual P-Channel Typical Characteristics

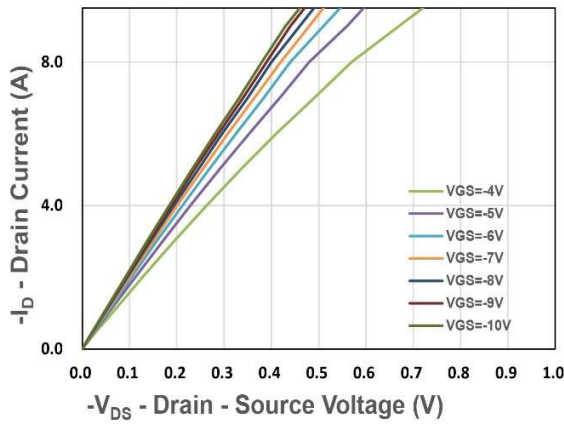


Figure 1. Output Characteristics

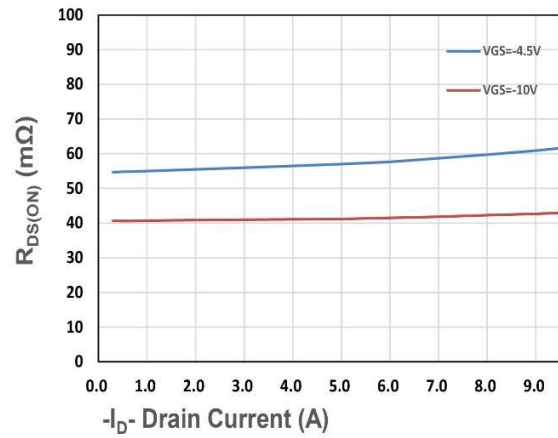


Figure 2. On-Resistance vs. ID

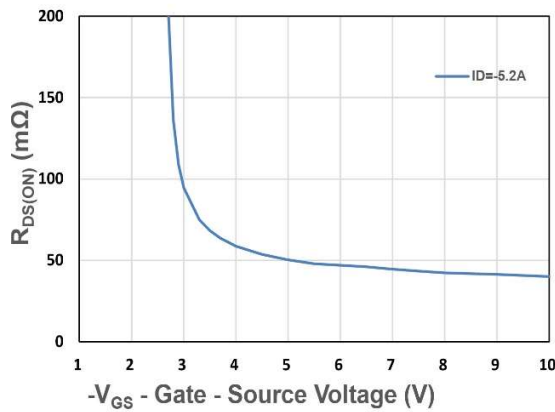


Figure 3. On-Resistance vs. VGS

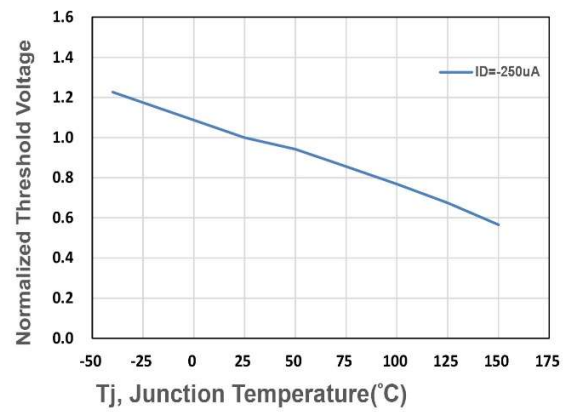


Figure 4. Gate Threshold Voltage

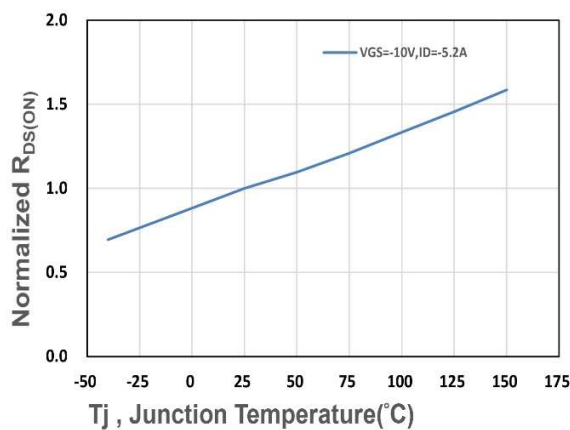


Figure 5. Drain-Source On Resistance

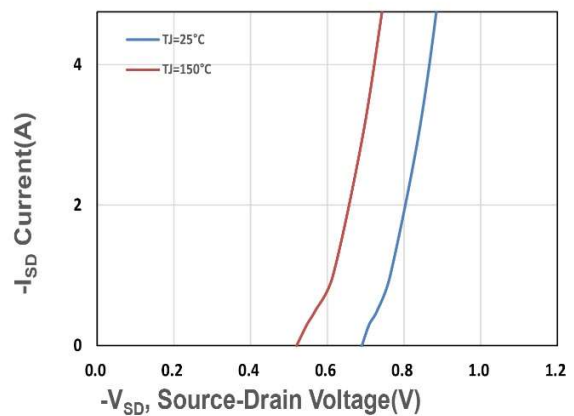
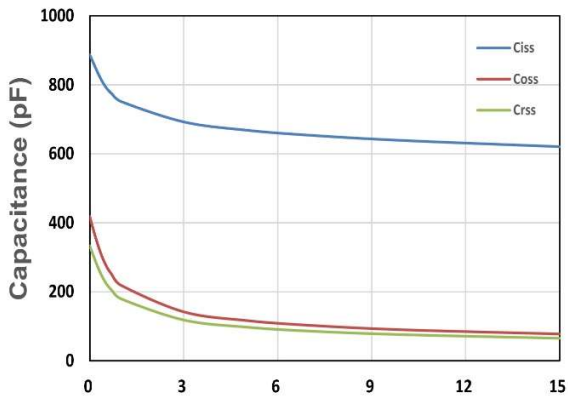


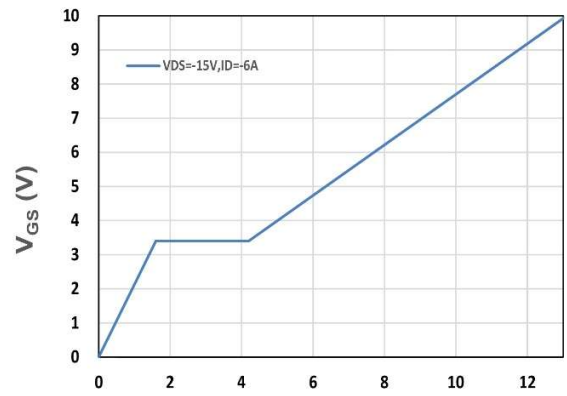
Figure 6. Source-Drain Diode Forward

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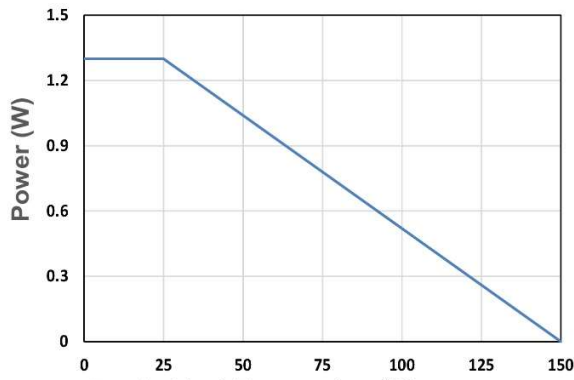
$-V_{DS}$ - Drain - Source Voltage (V)

Figure 7. Capacitance



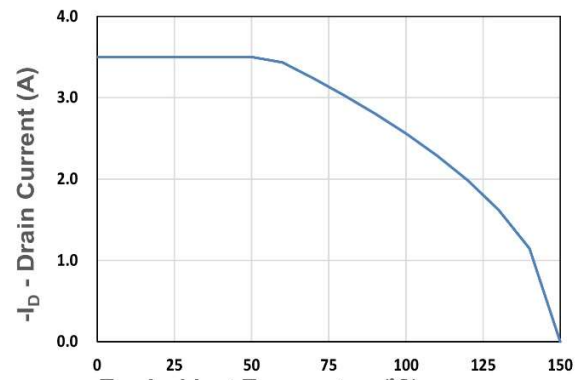
Q_g , Total Gate Charge (nC)

Figure 8. Gate Charge Characteristics



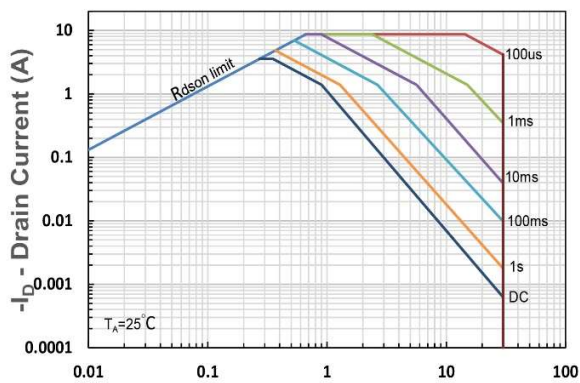
T_A - Ambient Temperature(°C)

Figure 9. Power Dissipation



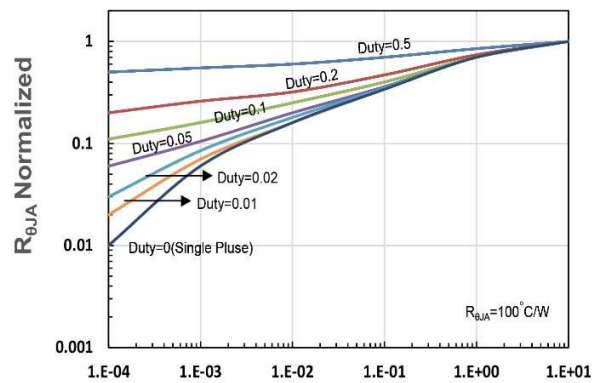
T_A - Ambient Temperature(°C)

Figure 10. Drain Current



$-V_{DS}$ - Drain-Source Voltage (V)

Figure 11. Safe Operating Area



t_1 , Square Wave Pulse Duration(s)

Figure 12. $R_{\theta JA}$ Transient Thermal Impedance