




# Power MOSFETS

## DATASHEET

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**LM20E80PGI3A**

P-Channel  
Enhancement Mode MOSFET

 Leadpower-semiconductor Corp., Ltd

 [sales@leadpower-semi.com](mailto:sales@leadpower-semi.com)

 (03) 6577339 FAX : (03) 6577229

 [www.leadpower-semi.com](http://www.leadpower-semi.com)



Quality Management Systems

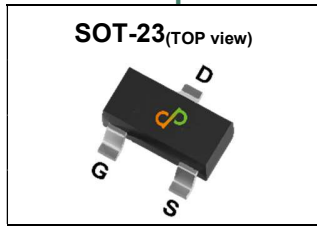
ISO 9001:2015 Certificate

# LM20E80PGI3A

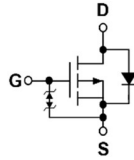


## P-Channel Enhancement Mode MOSFET

### Pin Description



### Symbol



### Product Summary

Symbol	P-Channel	Unit
$V_{DSS}$	-20	V
$R_{DS(ON)-Max}$	580	m $\Omega$
$I_D$	-0.64	A

### Feature

- Low Gate Charge(Qg)
- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- ESD Protection

### Applications

- Small Signal Switch
- Load Switch

### Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM20E80PGI3A	SOT-23	Tape & Reel	3000 / Tape & Reel	11□□□

Note : □□□ = Lot Code

### Absolute Maximum Ratings (T<sub>J</sub>=25°C Unless Otherwise Noted)

Symbol	Parameter	P-Channel	Unit	
$V_{DSS}$	Drain-Source Voltage	-20	V	
$V_{GSS}$	Gate-Source Voltage	±12		
$T_J$	Maximum Junction Temperature	150	°C	
$T_{STG}$	Storage Temperature Range	-55 to 150	°C	
$I_S$	Diode Continuous Forward Current	$T_A=25^\circ C$	-0.3	A
$I_{DM}^{(1)}$	Pulse Drain Current Tested	$T_A=25^\circ C$	-1.5	A
$I_D$	Continuous Drain Current	$T_A=25^\circ C$	-0.64	A
		$T_A=70^\circ C$	-0.51	
$P_D$	Maximum Power Dissipation	$T_A=25^\circ C$	0.35	W
		$T_A=70^\circ C$	0.22	

### Thermal Characteristics

Symbol	Parameter	Rating	Unit	
$R_{\theta JA}^{(2)}$	Thermal Resistance-Junction to Ambient	Steady State	350	°C/W

Note ① : Max. current is limited by junction temperature

Note ② : Surface Mounted on 1in<sup>2</sup> FR-4 board with 1oz

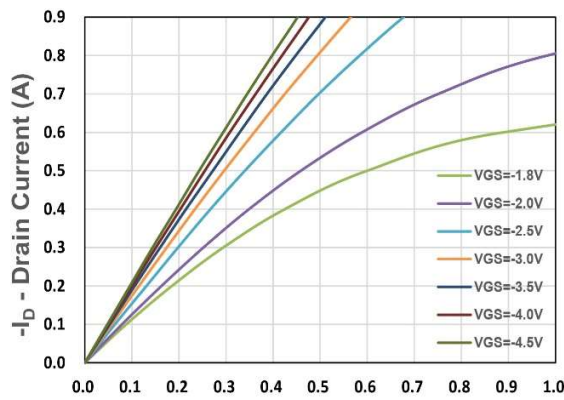
## P-Channel Electrical Characteristics (T<sub>J</sub>=25°C Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static Electrical Characteristics</b>						
<b>BV<sub>DSS</sub></b>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>DS</sub> =-250uA	-20	-	-	V
<b>I<sub>DSS</sub></b>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-16V, V <sub>GS</sub> =0V	-	-	-1	uA
<b>V<sub>GS(th)</sub></b>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>DS</sub> =-250uA	-0.5	-0.75	-1	V
<b>I<sub>GSS</sub></b>	Gate Leakage Current	V <sub>GS</sub> =±12V, V <sub>DS</sub> =0V	-	-	±10	uA
<b>R<sub>DS(ON)</sub></b> <sup>③</sup>	Drain-Source On-state Resistance	V <sub>GS</sub> =-4.5V, I <sub>DS</sub> =-550mA	-	482	580	mΩ
		V <sub>GS</sub> =-2.5V, I <sub>DS</sub> =-450mA	-	666	865	
		V <sub>GS</sub> =-1.8V, I <sub>DS</sub> =-350mA	-	1037	1556	
<b>gfs</b>	Forward Transconductance	V <sub>DS</sub> =-5V, I <sub>DS</sub> =-550mA	-	1	-	S
<b>Dynamic Characteristics</b> <sup>④</sup>						
<b>C<sub>iss</sub></b>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =10V, Freq.=1MHz	-	58	-	pF
<b>C<sub>oss</sub></b>	Output Capacitance		-	5.7	-	
<b>C<sub>rss</sub></b>	Reverse Transfer Capacitance		-	4.4	-	
<b>t<sub>d(ON)</sub></b>	Turn-on Delay Time	V <sub>GS</sub> =-4.5V, V <sub>DS</sub> =-10V, I <sub>D</sub> =-1A, R <sub>GEN</sub> =3Ω	-	0.4	-	nS
<b>t<sub>r</sub></b>	Turn-on Rise Time		-	0.03	-	
<b>t<sub>d(OFF)</sub></b>	Turn-off Delay Time		-	0.04	-	
<b>t<sub>f</sub></b>	Turn-off Fall Time		-	1.1	-	
<b>Q<sub>g</sub></b>	Total Gate Charge	V <sub>GS</sub> =-2.5V, V <sub>DS</sub> =-10V I <sub>D</sub> =-0.55A	-	0.6	-	nC
<b>Q<sub>g</sub></b>	Total Gate Charge	V <sub>GS</sub> =-4.5V, V <sub>DS</sub> =-10V, I <sub>D</sub> =-0.55A	-	1	-	
<b>Q<sub>gs</sub></b>	Gate-Source Charge		-	0.17	-	
<b>Q<sub>gd</sub></b>	Gate-Drain Charge		-	0.18	-	
<b>Source-Drain Characteristics</b>						
<b>V<sub>SD</sub></b> <sup>③</sup>	Diode Forward Voltage	I <sub>SD</sub> =-0.55A, V <sub>GS</sub> =0V	-	-0.75	-1.1	V

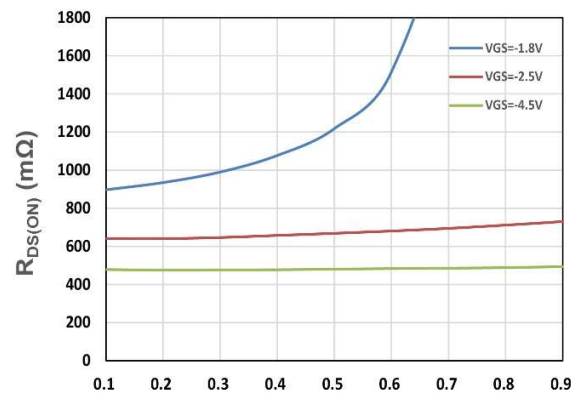
Note ③ : Pulse test (pulse width≤300us, duty cycle≤2%).

Note ④ : Guaranteed by design, not subject to production testing.

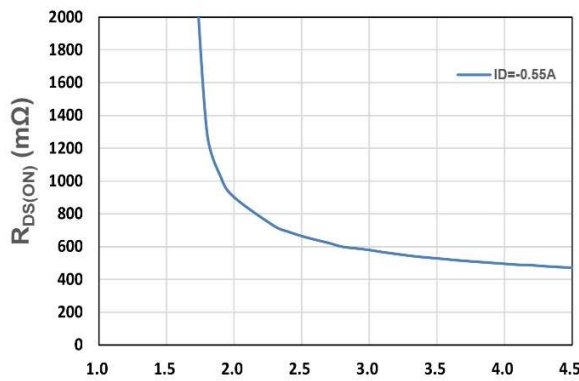
## P-Channel Typical Characteristics



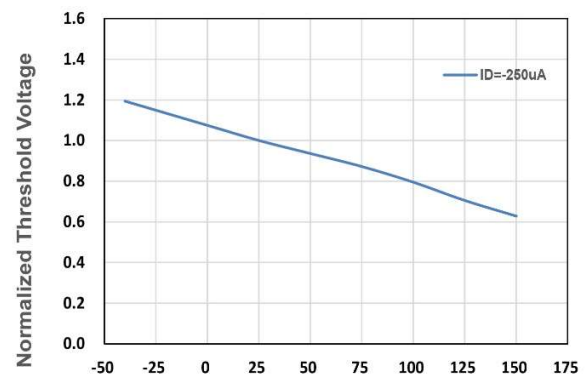
-V<sub>DS</sub> - Drain - Source Voltage (V)  
Figure 1. Output Characteristics



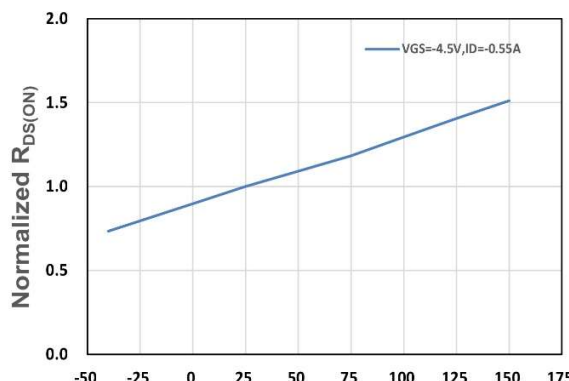
-ID - Drain Current (A)  
Figure 2. On-Resistance vs. ID



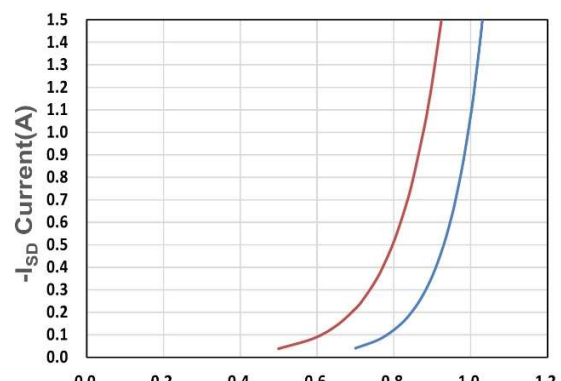
-V<sub>GS</sub> - Gate - Source Voltage (V)  
Figure 3. On-Resistance vs. VGS



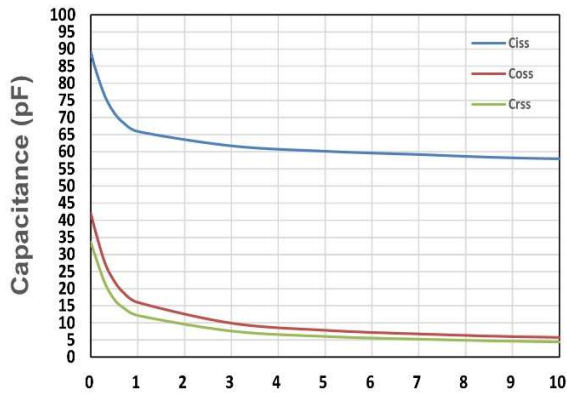
T<sub>j</sub>, Junction Temperature(°C)  
Figure 4. Gate Threshold Voltage



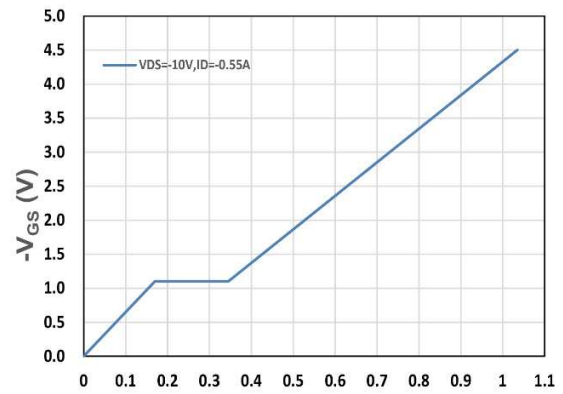
T<sub>j</sub>, Junction Temperature(°C)  
Figure 5. Drain-Source On Resistance



-V<sub>SD</sub>, Source-Drain Voltage(V)  
Figure 6. Source-Drain Diode Forward



$-V_{DS}$  - Drain - Source Voltage (V)  
Figure 7. Capacitance



Qg, Total Gate Charge (nC)  
Figure 8. Gate Charge Characteristics

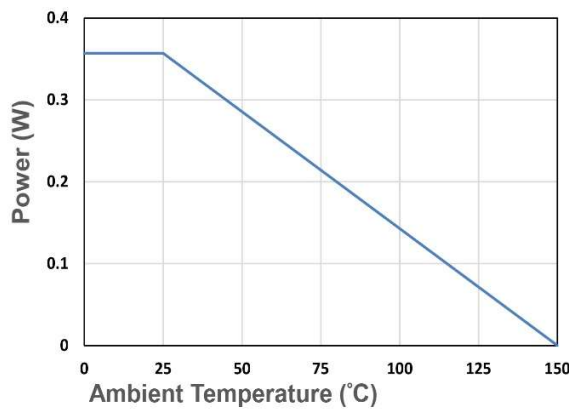


Figure 9. Power Dissipation

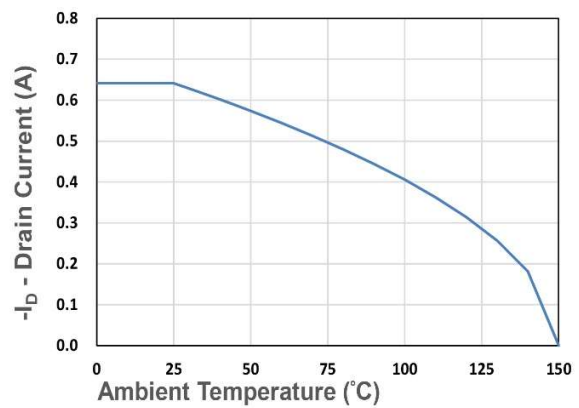


Figure 10. Drain Current

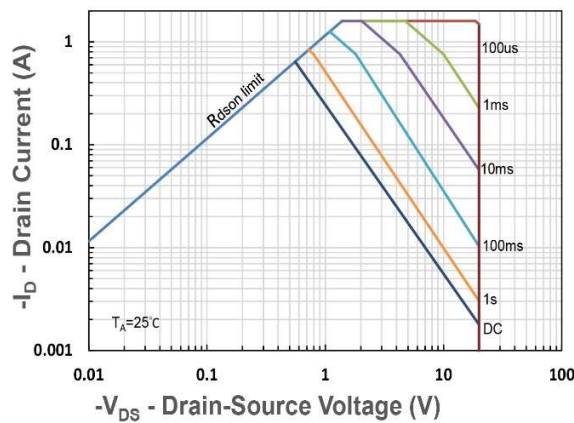


Figure 11. Safe Operating Area

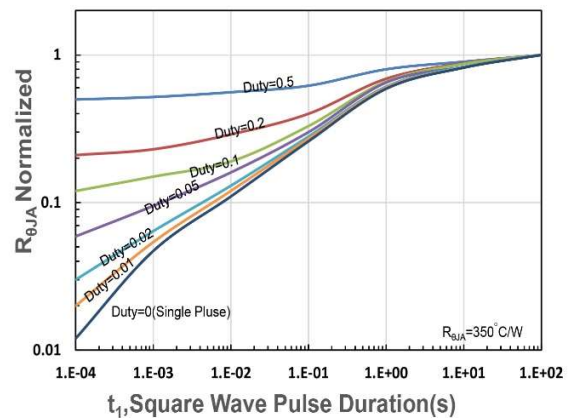


Figure 12.  $R_{\theta JA}$  Transient Thermal Impedance