# Power MOSFETS

## DATASHEET

## LM20B50DGE6A

Dual N-Channel

Enhancement Mode MOSFET

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Quality Management Systems

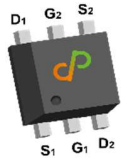
ISO 9001:2015 Certificate

# LM20B50DGE6A

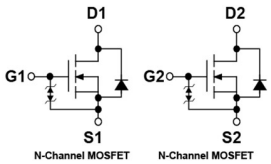
## Dual N-Channel Enhancement Mode MOSFET

### Pin Description

SOT-563 (TOP view)




Symbol




| Symbol | Dual N-Channel | Unit |
|---|---|---|
| $V_{DSS}$ | 20 | V |
| $R_{DS(ON)\text{-}max}$ | 250 | mΩ |
| $I_D$ | 1 | A |

### Feature

- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- ESD Protection

### Applications

- Power Management in DC/DC Converters
- Load Switch

### Ordering Information

| Orderable Part Number | Package Type | Form | Shipping | Marking |
|---|---|---|---|---|
| LM20B50DGE6A | SOT-563 | Tape & Reel | 3000 / Tape & Reel | 1□□□ |

Note：□□□= Lot Code

### Absolute Maximum Ratings ($T_J$=25°C Unless Otherwise Noted)

| Symbol | Parameter | | Dual N-Channel | Unit |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 20 | V |
| $V_{GSS}$ | Gate-Source Voltage | | ±12 | |
| $T_J$ | Maximum Junction Temperature | | 150 | °C |
| $T_{STG}$ | Storage Temperature Range | | -55 to 150 | °C |
| $I_{DM}$① | Pulse Drain Current Tested | $T_A$=25°C | 1 | A |
| $I_D$ | Continuous Drain Current | $T_A$=25°C | 1① | A |
| | | $T_A$=70°C | 0.84 | |
| $P_D$ | Maximum Power Dissipation | $T_A$=25°C | 0.42 | W |
| | | $T_A$=70°C | 0.27 | |

### Thermal Characteristics

| Symbol | Parameter | | Rating | Unit |
|---|---|---|---|---|
| $R_{\theta JA}$③ | Thermal Resistance-Junction to Ambient | Steady State | 300 | °C/W |

Note ①：Max. current is limited by bonding wire.
Note ②：UIS tested and pulse width are limited by maximum junction temperature 150°C
Note ③：Surface Mounted on 1in$^2$ FR-4 board with 1oz.

## Dual N-Channel Electrical Characteristics ($T_J$=25°C Unless Otherwise Noted)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Static Electrical Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$=0V, $I_{DS}$=250uA | 20 | - | - | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$=16V, $V_{GS}$=0V | - | - | 1 | uA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$, $I_{DS}$=250uA | 0.5 | 0.75 | 1 | V |
| $I_{GSS}$ | Gate Leakage Current | $V_{GS}$=±12V, $V_{DS}$=0V | - | - | ±10 | uA |
| $R_{DS(ON)}$④ | Drain-Source On-state Resistance | $V_{GS}$=4.5V, $I_{DS}$=0.6A | - | 220 | 250 | mΩ |
| | | $V_{GS}$=2.5V, $I_{DS}$=0.4A | - | 280 | 365 | |
| | | $V_{GS}$=1.8V, $I_{DS}$=0.35A | - | 390 | 585 | |
| **gfs** | Forward Transconductance | $V_{DS}$=3V, $I_{DS}$=0.3A | - | 1.3 | - | S |
| **Dynamic Characteristics** ⑤ | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{GS}$=0V, $V_{DS}$=10V, Freq.=1MHz | - | 40 | - | pF |
| $C_{oss}$ | Output Capacitance | | - | 16.5 | - | |
| $C_{rss}$ | Reverse Transfer Capacitance | | - | 10.1 | - | |
| $td_{(ON)}$ | Turn-on Delay Time | $V_{GS}$=4.5V,$V_{DS}$=10V, $I_D$=2A,$R_{GEN}$=6Ω | - | 1.2 | - | nS |
| $t_r$ | Turn-on Rise Time | | - | 24.6 | - | |
| $t_{d(OFF)}$ | Turn-off Delay Time | | - | 13.5 | - | |
| $t_f$ | Turn-off Fall Time | | - | 14.6 | - | |
| $Q_g$ | Total Gate Charge | $V_{GS}$=2.5V,$V_{DS}$=10V $I_D$=0.6A | - | 0.55 | - | nC |
| $Q_g$ | Total Gate Charge | $V_{GS}$=4.5V,$V_{DS}$=10V, $I_D$=0.6A | - | 1 | - | |
| $Q_{gs}$ | Gate-Source Charge | | - | 0.31 | - | |
| $Q_{gd}$ | Gate-Drain Charge | | - | 0.11 | - | |
| **Source-Drain Characteristics** | | | | | | |
| $V_{SD}$④ | Diode Forward Voltage | $I_{SD}$=0.3A, $V_{GS}$=0V | - | 0.75 | 1.1 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_F$=0.3A, $V_R$=10V dI$_F$/dt=100A/μs | - | 9 | - | nS |
| $Q_{rr}$ | Reverse Recovery Charge | | - | 0.78 | - | nC |

Note ④ : Pulse test (pulse width≤300us, duty cycle≤2%).
Note ⑤ : Guaranteed by design, not subject to production testing.

## Dual N-Channel Typical Characteristics

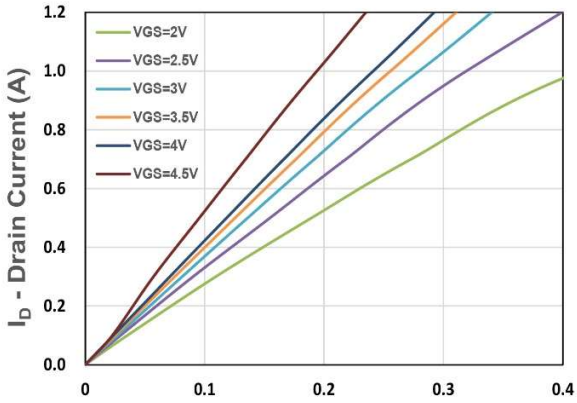



Figure 1. Output Characteristics

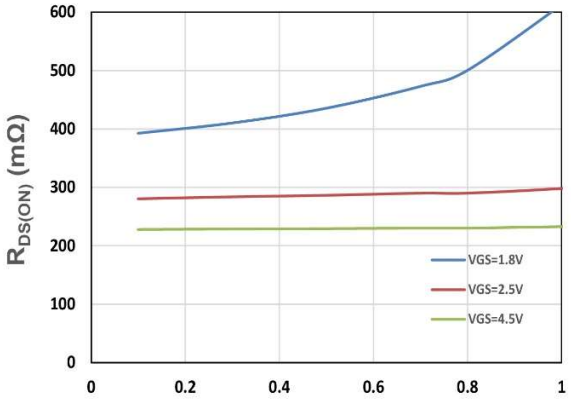



Figure 2. On-Resistance vs. ID

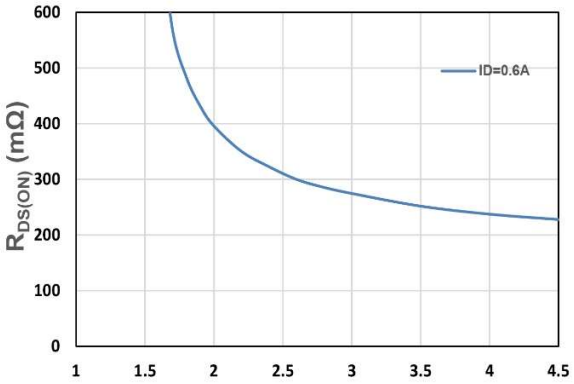



Figure 3. On-Resistance vs. VGS

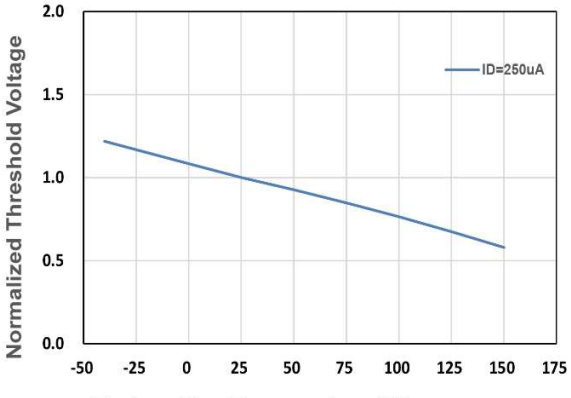



Figure 4. Gate Threshold Voltage

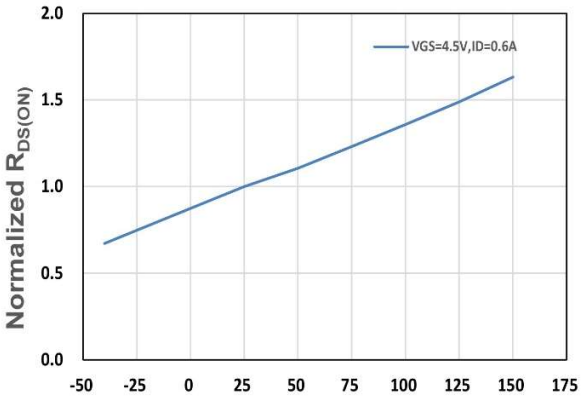



Figure 5. Drain-Source On Resistance

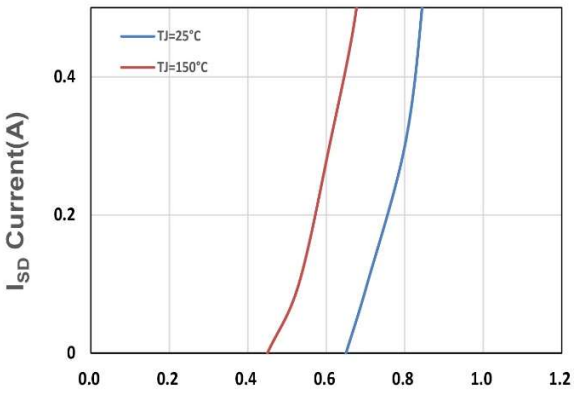
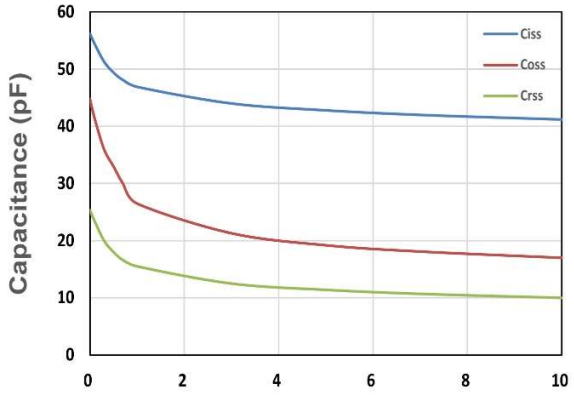
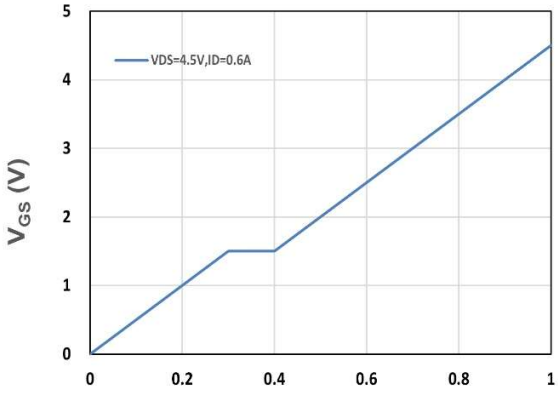



Figure 6. Source-Drain Diode Forward



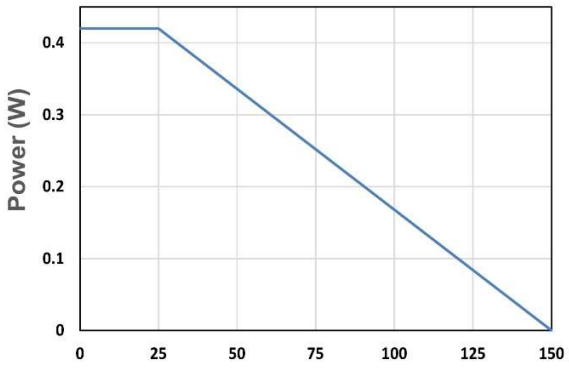

$V_{DS}$ - Drain - Source Voltage (V)

Figure 7. Capacitance



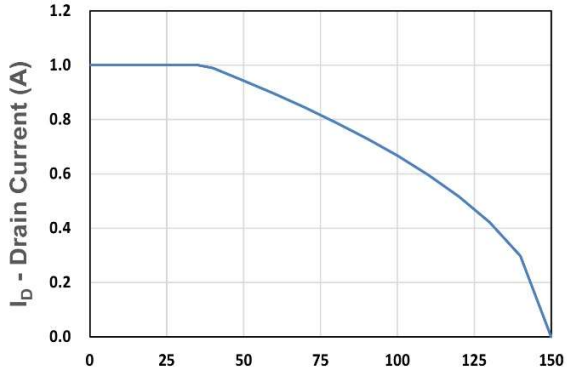

Qg, Total Gate Charge (nC)

Figure 8. Gate Charge Characteristics



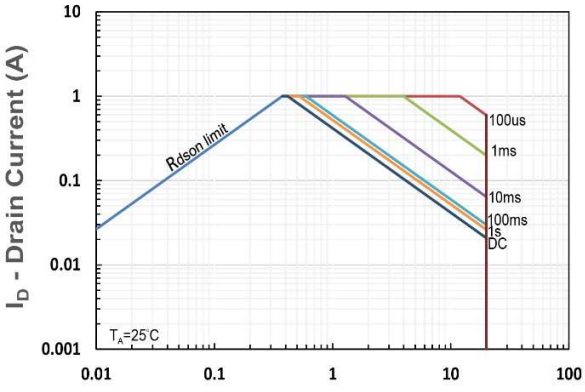

$T_A$ - Junction Temperature (°C)

Figure 9. Power Dissipation



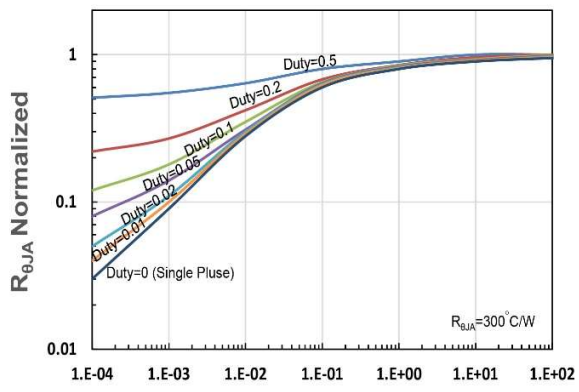

$T_A$ - Junction Temperature (°C)

Figure 10. Drain Current




$V_{DS}$ - Drain-Source Voltage (V)

Figure 11. Safe Operating Area




$t_1$,Square Wave Pulse Duration(s)

Figure 12. RθJA Transient Thermal Impedance