Power MOSFETS

DATASHEET

LM30072PAP3A

P-Channel

Enhancement Mode MOSFET

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Quality Management Systems

ISO 9001:2015 Certificate

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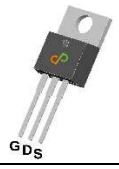
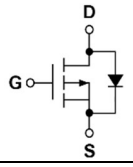
P-Channel Enhancement Mode MOSFET

Pin Description

TO-220-3L (TOP view)	Symbol
	

Ordering Information

Symbol	P-Channel	Unit
V_{DSS}	-30	V
$R_{DS(ON)-Max}$	8	mΩ
I_D	-102	A

Feature

- Low Rdson application
- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- 100% UIS Tested and Rg Tested

Applications

- DC-DC converters
- Battery Powered System

Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM30072PAP3A	TO-220-3L	Tube	50 / Tape & Reel	30072 □□□□□□

Note：□□□□□□ = Lot Code

Absolute Maximum Ratings (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter		P-Channel	Unit
V_{DSS}	Drain-Source Voltage		-30	V
V_{GSS}	Gate-Source Voltage		±20	
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature Range		-55 to 150	°C
I_{DM}①	Pulse Drain Current Tested	T_C=25°C	-255	A
I_D	Continuous Drain Current	T_C=25°C	-102	A
		T_C=100°C	-65	
P_D	Maximum Power Dissipation	T_C=25°C	83	W
		T_C=100°C	33	
I_D	Continuous Drain Current	T_A=25°C	-16	A
		T_A=70°C	-13	
P_D	Maximum Power Dissipation	T_A=25°C	2	W
		T_A=70°C	1.3	
I_{AS}②	Avalanche Current, Single pulse	L=0.1mH	-33	A
		L=0.5mH	-15	
E_{AS}②	Avalanche Energy, Single pulse	L=0.1mH	54	mJ
		L=0.5mH	56	

Thermal Characteristics

Symbol	Parameter		Rating	Unit
$R_{\theta JC}$	Thermal Resistance-Junction to Case	Steady State	1.5	°C/W
$R_{\theta JA}$③	Thermal Resistance-Junction to Ambient	Steady State	62.5	°C/W

Note ①：Max. current is limited by junction temperature

Note ②：UIS tested and pulse width are limited by maximum junction temperature 150°C.

Note ③：Surface Mounted on 1in^2 FR-4 board with 1oz.

P-Channel Electrical Characteristics (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Electrical Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_{DS}=-250uA	-30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-24V, V_{GS}=0V	-	-	-1	uA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_{DS}=-250uA	-1	-1.5	-2	V
I_{GSS}	Gate Leakage Current	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
$R_{DS(ON)}$④	Drain-Source On-state Resistance	V_{GS}=-10V, I_{DS}=-12A	-	6.5	8	mΩ
		V_{GS}=-4.5V, I_{DS}=-9A	-	8.2	10.7	
gfs	Forward Transconductance	V_{DS}=-5V, I_{DS}=-12A	-	35	-	S
Dynamic Characteristics ⑤						
R_G	Gate Resistance	V_{GS}=0V,V_{DS}=0V, Freq.=1MHz	-	11	-	Ω
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-15V, Freq.=1MHz	-	4435	-	pF
C_{oss}	Output Capacitance		-	500	-	
C_{rss}	Reverse Transfer Capacitance		-	373	-	
$td_{(ON)}$	Turn-on Delay Time	V_{GS}=-10V,V_{DS}=-15V, I_D=-1A,R_{GEN}=3Ω	-	51	-	nS
t_r	Turn-on Rise Time		-	40	-	
$t_{d(OFF)}$	Turn-off Delay Time		-	77	-	
t_f	Turn-off Fall Time		-	56	-	
Q_g	Total Gate Charge	V_{GS}=-4.5V,V_{DS}=-15V I_D=-10A	-	42	-	nC
Q_g	Total Gate Charge	V_{GS}=-10V,V_{DS}=-15V, I_D=-10A	-	88	-	
Q_{gs}	Gate-Source Charge		-	14	-	
Q_{gd}	Gate-Drain Charge		-	8.6	-	
Source-Drain Characteristics						
V_{SD}④	Diode Forward Voltage	I_{SD}=-3.6A, V_{GS}=0V	-	-0.75	-1.1	V
t_{rr}	Reverse Recovery Time	I_F=-3.6A, V_R=-10V dI$_F$/dt=100A/μs	-	25	-	nS
Q_{rr}	Reverse Recovery Charge		-	15	-	nC

Note ④：Pulse test (pulse width≤300us, duty cycle≤2%).
Note ⑤：Guaranteed by design, not subject to production testing.

P-Channel Typical Characteristics

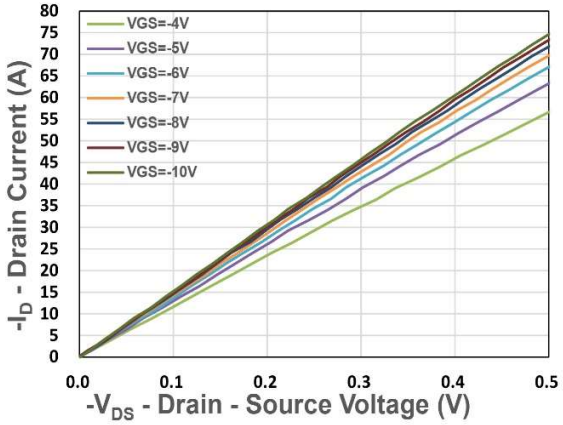


Figure 1. Output Characteristics

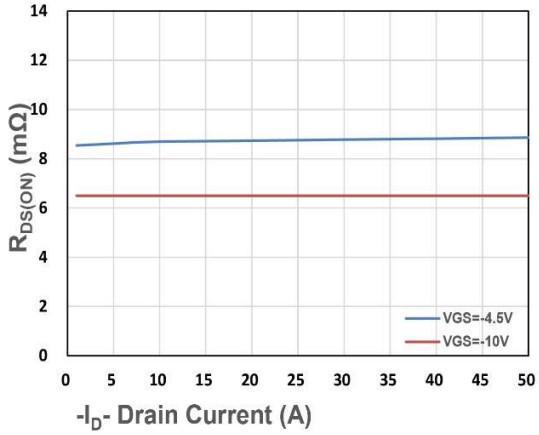


Figure 2. On-Resistance vs. ID

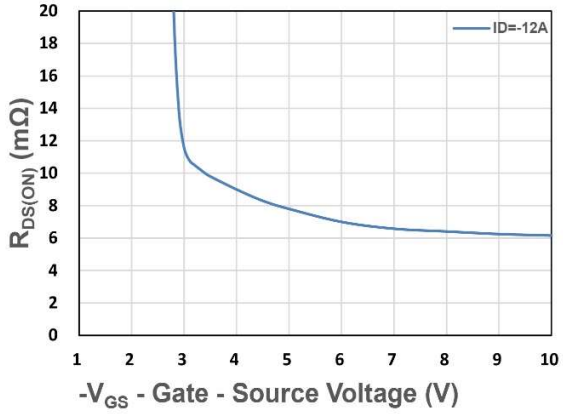


Figure 3. On-Resistance vs. VGS

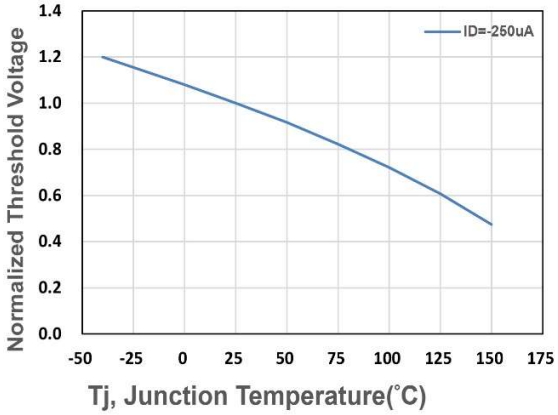


Figure 4. Gate Threshold Voltage

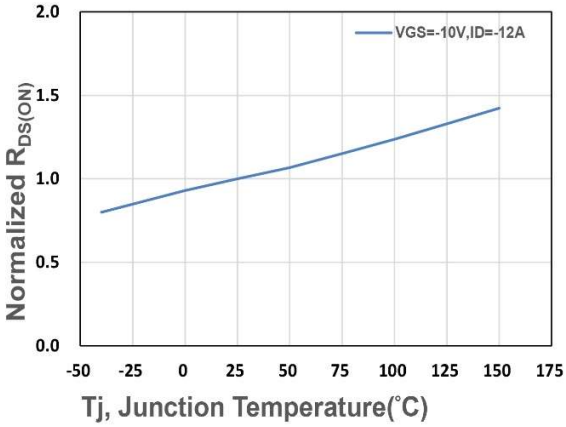


Figure 5. Drain-Source On Resistance

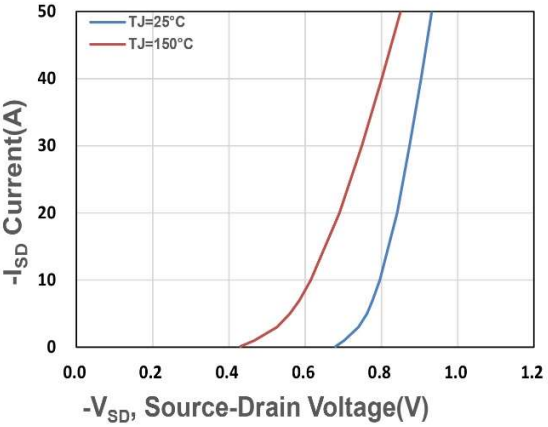


Figure 6. Source-Drain Diode Forward

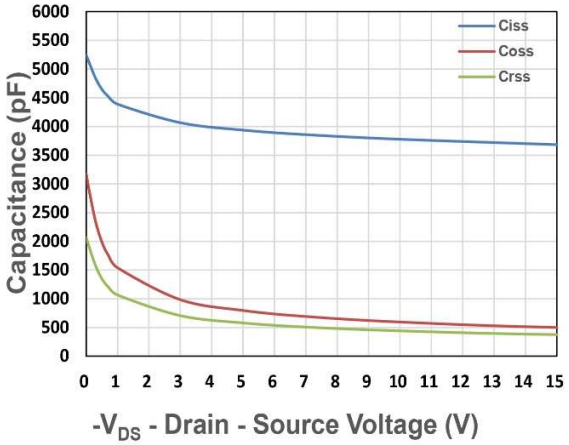


Figure 7. Capacitance

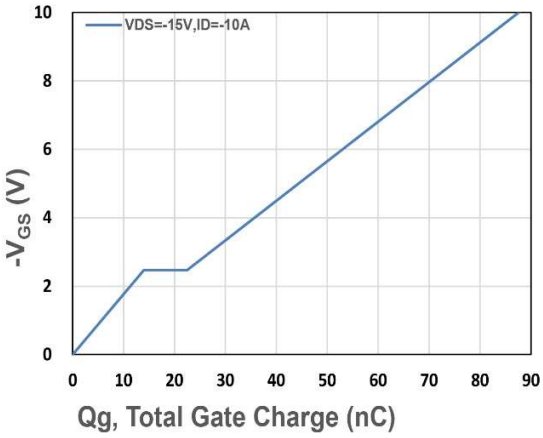


Figure 8. Gate Charge Characteristics

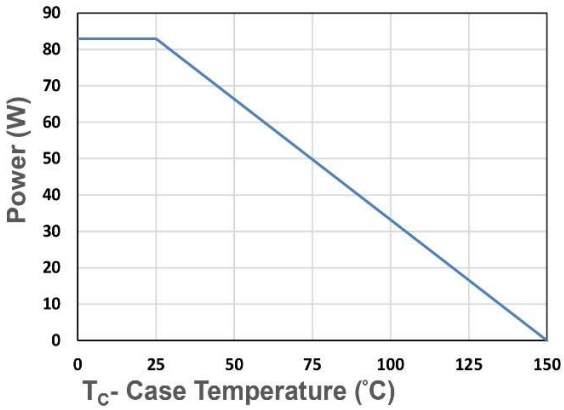


Figure 9. Power Dissipation

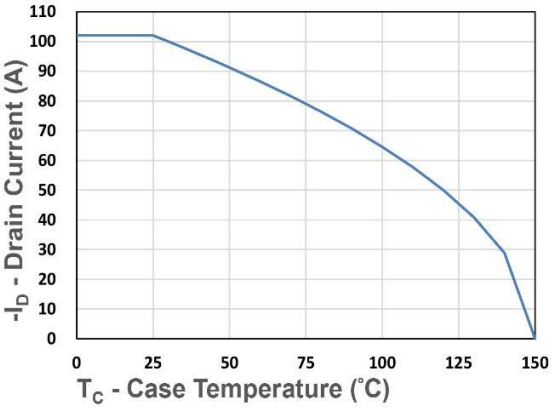


Figure 10. Drain Current

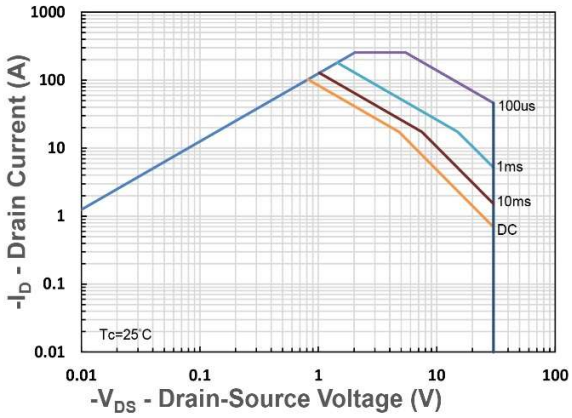


Figure 11. Safe Operating Area

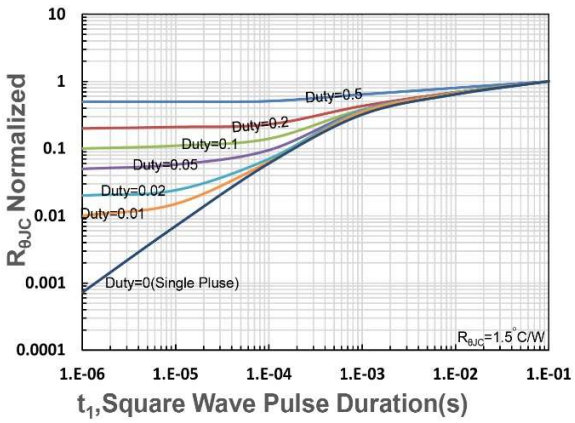


Figure 12. RθJC Transient Thermal Impedance