





Power MOSFETS

PRELIMINARY DATASHEET

LM65028NAK8A

N-Channel
Enhancement Mode MOSFET

 Leadpower-semiconductor Corp., Ltd

 sales@leadpower-semi.com

 (03) 6577339 FAX : (03) 6577229

 www.leadpower-semi.com

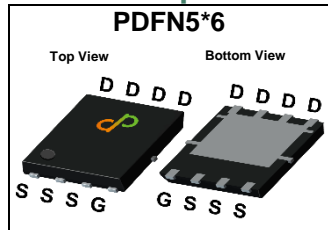


Quality Management Systems

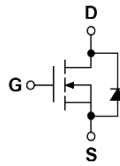
ISO 9001:2015 Certificate

N-Channel Enhancement Mode MOSFET

Pin Description



Symbol



Product Summary

Symbol	N-Channel	Unit
V_{DSS}	65	V
$R_{DS(ON)-Max}$	2.8	m Ω
ID	142	Alm

Feature

- Fast switching speed
- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- 100% UIS and Rg Tested

Applications

- Hard Switching and High Speed Circuit
- DC/DC in Telecoms and Industrial

Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM65028NAK8A	PDFN5*6	Tape & Reel	5000 / Tape & Reel	65028 □□□□□□

Note : □□□□□□ = Lot Code

Absolute Maximum Ratings (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter	N-Channel	Unit
V_{DSS}	Drain-Source Voltage	65	V
V_{GSS}	Gate-Source Voltage	±20	
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-55 to 150	°C
I_S	Diode Continuous Forward Current	$T_C=25^\circ\text{C}$ 79	A
I_{DM}	Pulse Drain Current Tested	$T_C=25^\circ\text{C}$ 400	
I_D	Continuous Drain Current	$T_C=25^\circ\text{C}$ 142 ^①	A
		$T_C=100^\circ\text{C}$ 111	
P_D	Maximum Power Dissipation	$T_C=25^\circ\text{C}$ 87	W
		$T_C=100^\circ\text{C}$ 35	
I_D	Continuous Drain Current	$T_A=25^\circ\text{C}$ 26	A
		$T_A=70^\circ\text{C}$ 21	
P_D	Maximum Power Dissipation	$T_A=25^\circ\text{C}$ 1.9	W
		$T_A=70^\circ\text{C}$ 1.2	
I_{AS} ^②	Avalanche Current, Single pulse	$L=0.1\text{mH}$ 40	A
E_{AS} ^②	Avalanche Energy, Single pulse	$L=0.1\text{mH}$ 80	mJ

Thermal Characteristics

Symbol	Parameter	Rating	Unit
$R_{\theta JC}$	Thermal Resistance-Junction to Case	Steady State	1.44
$R_{\theta JA}$ ^③	Thermal Resistance-Junction to Ambient	Steady State	65

Note ① : Max. current is limited by bonding wire

Note ② : UIS tested and pulse width are limited by maximum junction temperature 150°C

Note ③ : Surface Mounted on 1in² FR-4 board with 1oz.

N-Channel Electrical Characteristics (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Electrical Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =250uA	65	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V _{DS} =52V, V _{GS} =0V	-	-	1	uA
V_{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =250uA	1	1.6	2.4	V
I_{GSS}	Gate Leakage Current	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
R_{DS(ON)}^④	Drain-Source On-state Resistance	V _{GS} =10V, I _{DS} =20A	-	2.3	2.8	mΩ
		V _{GS} =4.5V, I _{DS} =20A	-	3.3	4.2	
gfs	Forward Transconductance	V _{DS} =5V, I _{DS} =20A	-	70	-	S
Dynamic Characteristics[®]						
R_G	Gate Resistance	V _{GS} =0V, V _{DS} =0V, Freq.=1MHz	-	1.3	-	Ω
C_{ISS}	Input Capacitance	V _{GS} =0V, V _{DS} =30V, Freq.=1MHz	-	4020	-	pF
C_{OSS}	Output Capacitance					
C_{rSS}	Reverse Transfer Capacitance					
td(ON)	Turn-on Delay Time	V _{GS} =10V, V _{DS} =30V, I _D =1A, R _{GEN} =6Ω	-	14	-	nS
t_r	Turn-on Rise Time					
t_{d(OFF)}	Turn-off Delay Time					
t_f	Turn-off Fall Time					
Q_g	Total Gate Charge	V _{GS} =4.5V, V _{DS} =30V, I _D =20A	-	35	-	nC
Q_g	Total Gate Charge	V _{GS} =10V, V _{DS} =30V, I _D =20A	-	69	-	
Q_{gs}	Gate-Source Charge		-	8	-	
Q_{gd}	Gate-Drain Charge		-	14	-	
Source-Drain Characteristics						
V_{SD}^④	Diode Forward Voltage	I _{SD} =20A, V _{GS} =0V	-	0.9	1.1	V
t_{rr}	Reverse Recovery Time	I _F =20A, V _R =30V	-	50	-	nS
Q_{rr}	Reverse Recovery Charge	dI _F /dt=100A/μs	-	44.5	-	nC

Note ④ : Pulse test (pulse width≤300us, duty cycle≤2%).

Note ⑤ : Guaranteed by design, not subject to production testing.

N-Channel Typical Characteristics

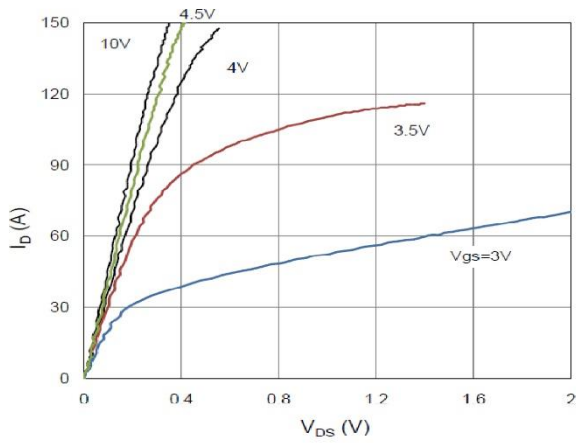


Figure 1. Output Characteristics

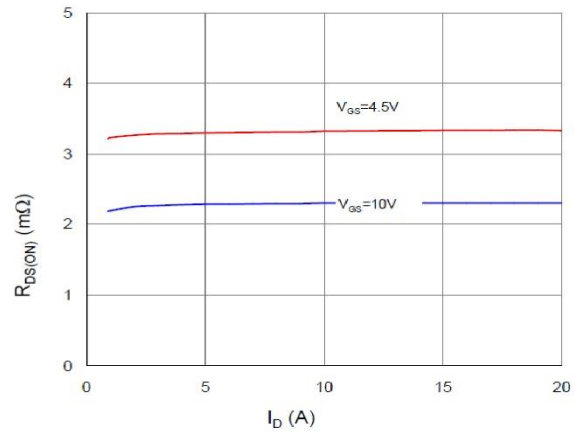


Figure 2. On-Resistance vs. I_D

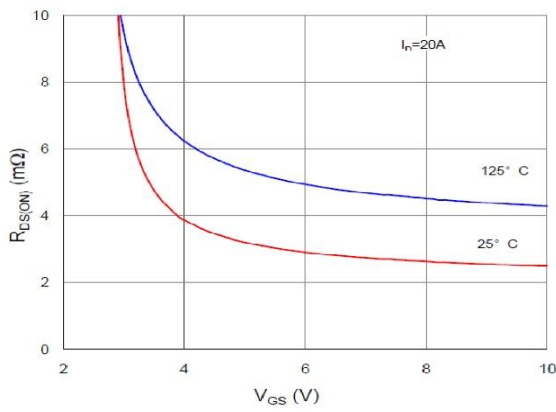


Figure 3. On-Resistance vs. V_{GS}

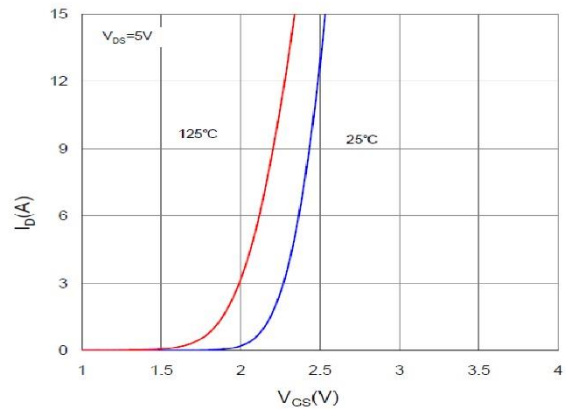


Figure 4. Gate Threshold Voltage

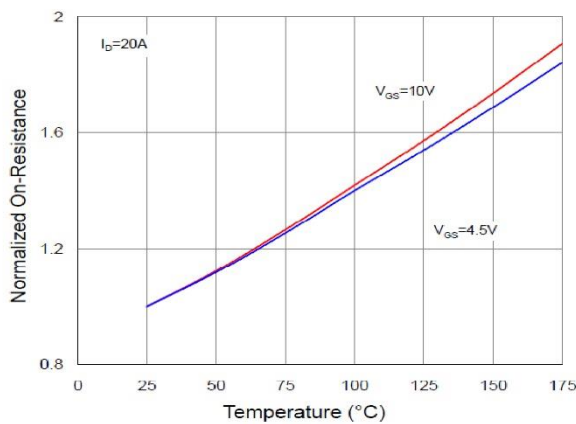


Figure 5. Drain-Source On Resistance

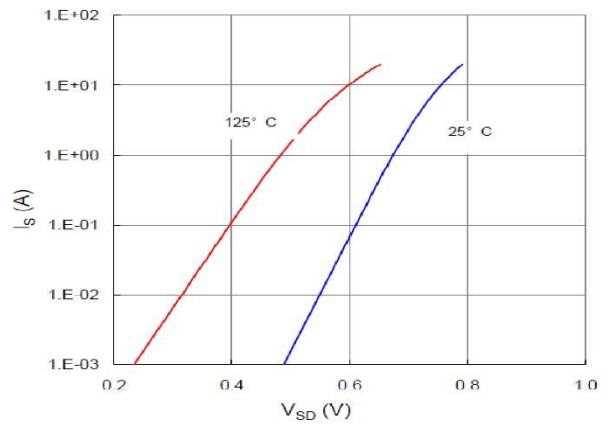


Figure 6. Source-Drain Diode Forward

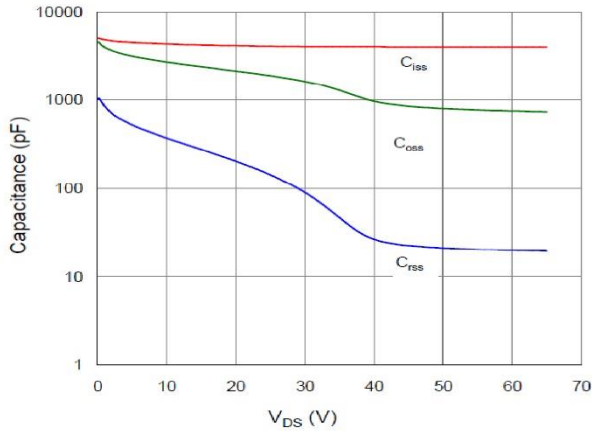


Figure 7. Capacitance

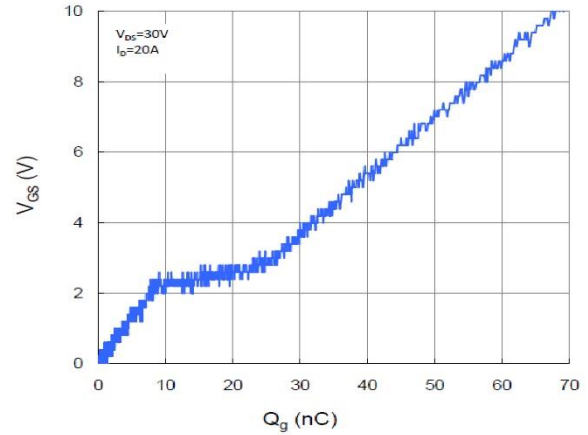


Figure 8. Gate Charge Characteristics

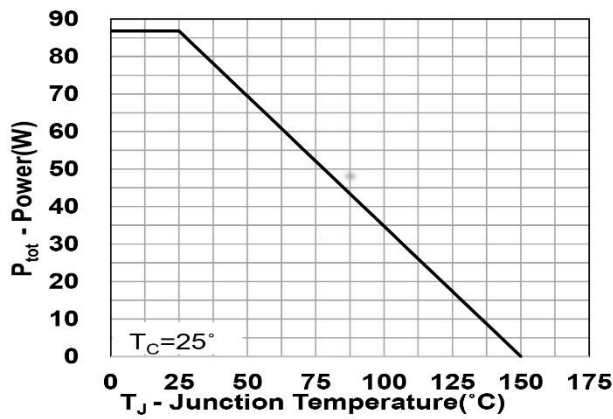


Figure 9. Power Dissipation

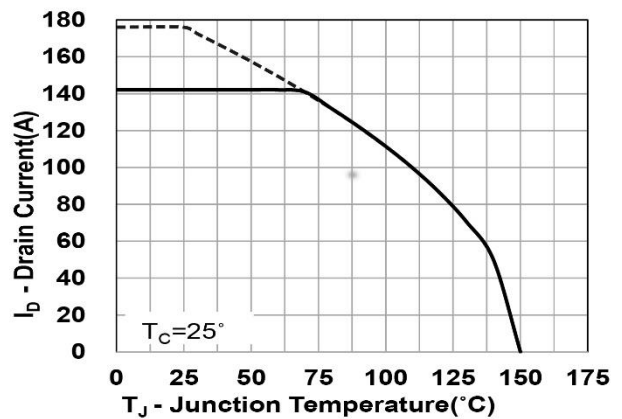


Figure 10. Drain Current

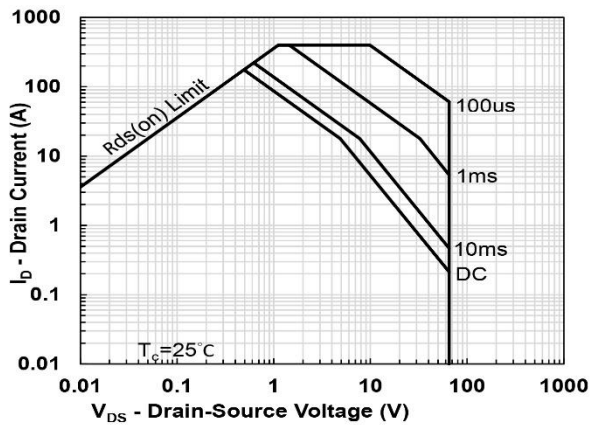


Figure 11. Safe Operating Area

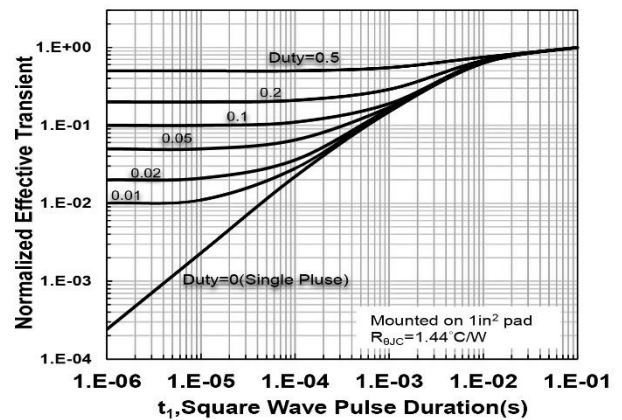


Figure 12. $R_{\theta JC}$ Transient Thermal Impedance