



Power MOSFETS

DATASHEET

LM20A10NGI3A

N-Channel
Enhancement Mode MOSFET

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Quality Management Systems
ISO 9001:2015 Certificate

-Channel Enhancement Mode MOSFET

Pin Description

SOT-23 (TOP view)	Symbol	Symbol	N-Channel	Unit
			V _{DSS}	20
			R _{DSON} -Max	85
			I _D	2.6

Feature

- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- ESD Protected

Product Summary

Applications

- Load Switch

Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM20A10NGI3A	SOT-23	Tape & Reel	3000 / Tape & Reel	20A10 <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>

Note: = Lot code

Absolute Maximum Ratings (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter	N-Channel	Unit
V _{DSS}	Drain-Source Voltage	20	V
V _{GSS}	Gate-Source Voltage	±8	
T _J	Maximum Junction Temperature	150	°C
T _{STG}	Storage Temperature Range	-55 to 150	°C
I _S	Diode Continuous Forward Current	T _A =25°C 0.7	A
I _{DM} ^①	Pulse Drain Current Tested	T _A =25°C 6.5	A
I _D ^②	Continuous Drain Current	T _A =25°C 2.6 T _A =70°C 2.1	A
P _D ^②	Maximum Power Dissipation	T _A =25°C 0.9 T _A =70°C 0.6	W
I _{AS} ^③	Avalanche Current, Single pulse	L=0.1mH 4 L=0.5mH 2	A
E _{AS} ^③	Avalanche Energy, Single pulse	L=0.1mH 0.8 L=0.5mH 1	mJ

Thermal Characteristics

Symbol	Parameter	Rating	Unit
R _{θJA} ^②	Thermal Resistance-Junction to Ambient	Steady State 140	°C/W

Note ① : Max. current is limited by junction temperature.

Note ② : Surface Mounted on 1in² FR-4 board with 1oz.

Note ③ : UIS tested and pulse width are limited by maximum junction temperature 150°C.

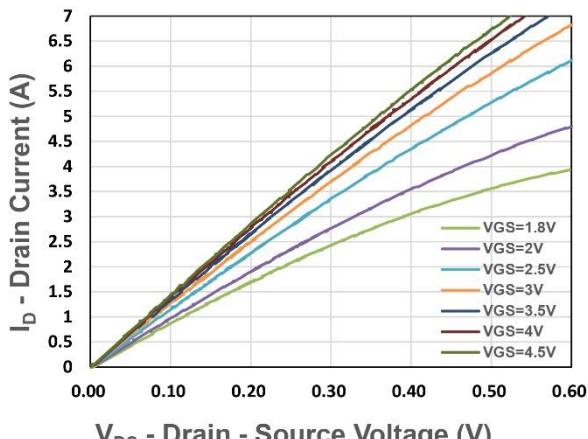
N-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Electrical Characteristics						
$\mathbf{BV_{DSS}}$	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}, I_{DS}=250\mu\text{A}$	20	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=16\text{V}, V_{GS}=0\text{V}$	-	-	1	μA
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_{DS}=250\mu\text{A}$	0.3	0.7	1	V
I_{GSS}	Gate Leakage Current	$V_{GS}=\pm 8\text{V}, V_{DS}=0\text{V}$	-	-	± 10	μA
$R_{DS(\text{ON})}^{\text{(1)}}$	Drain-Source On-state Resistance	$V_{GS}=4.5\text{V}, I_{DS}=2\text{A}$	-	70	85	$\text{m}\Omega$
		$V_{GS}=2.5\text{V}, I_{DS}=1.5\text{A}$		85	110	
		$V_{GS}=1.8\text{V}, I_{DS}=0.5\text{A}$	-	100	150	
g_{fs}	Forward Transconductance	$V_{DS}=5\text{V}, I_{DS}=1.6\text{A}$	-	4.5	-	S
Dynamic Characteristics ⁽⁵⁾						
R_G	Gate Resistance	$V_{GS}=0\text{V}, V_{DS}=0\text{V},$ Freq.=1MHz	-	4	-	Ω
C_{iss}	Input Capacitance	$V_{GS}=0\text{V},$ $V_{DS}=10\text{V},$ Freq.=1MHz	-	141	-	pF
C_{oss}	Output Capacitance		-	27	-	
C_{rss}	Reverse Transfer Capacitance		-	22	-	
$t_{d(\text{ON})}$	Turn-on Delay Time	$V_{GS}=4.5\text{V}, V_{DS}=10\text{V},$ $I_D=1\text{A}, R_{GEN}=1\Omega$	-	4.3	-	nS
t_r	Turn-on Rise Time		-	27	-	
$t_{d(\text{OFF})}$	Turn-off Delay Time		-	8	-	
t_f	Turn-off Fall Time		-	2.5	-	
Q_g	Total Gate Charge	$V_{GS}=2.5\text{V}, V_{DS}=10\text{V}$ $I_D=2\text{A}$	-	1.1	-	nC
Q_g	Total Gate Charge	$V_{GS}=4.5\text{V}, V_{DS}=10\text{V},$ $I_D=2\text{A}$	-	1.88	-	
Q_{gs}	Gate-Source Charge		-	0.42	-	
Q_{gd}	Gate-Drain Charge		-	0.34	-	
Source-Drain Characteristics						
$V_{SD}^{\text{(2)}}$	Diode Forward Voltage	$I_{SD}=1.6\text{A}, V_{GS}=0\text{V}$	-	0.7	1.1	V
t_{rr}	Reverse Recovery Time	$I_F=3\text{A}, V_R=20\text{V}$	-	4.3	-	nS
Q_{rr}	Reverse Recovery Charge	$dI_F/dt=100\text{A}/\mu\text{s}$	-	0.9	-	nC

Note ① : Pulse test (pulse width $\leq 300\text{us}$, duty cycle $\leq 2\%$).

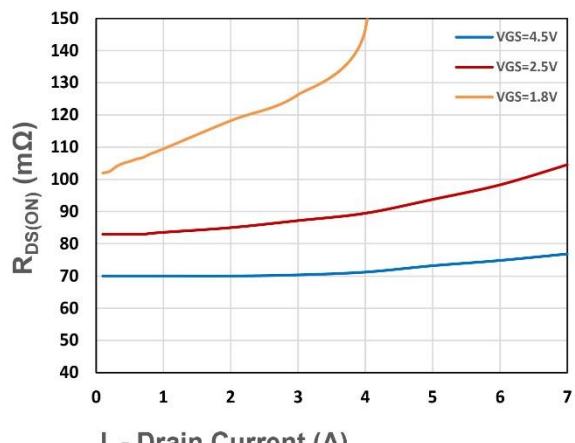
Note ⑤ : Guaranteed by design, not subject to production testing.

N-Channel Typical Characteristics



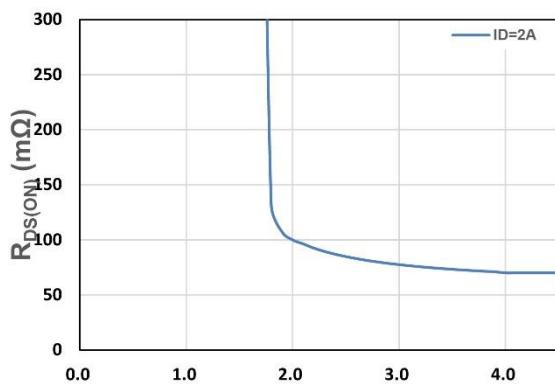
V_{DS} - Drain - Source Voltage (V)

Figure 1. Output Characteristics



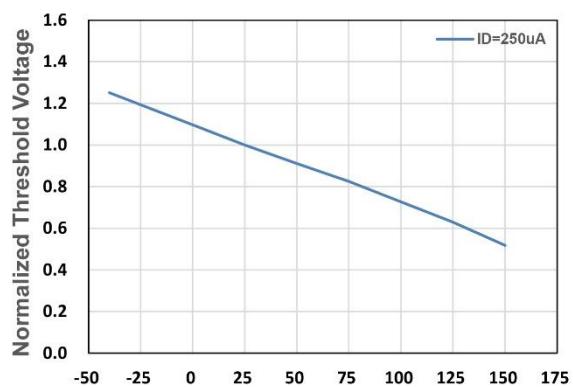
I_D - Drain Current (A)

Figure 2. On-Resistance vs. ID



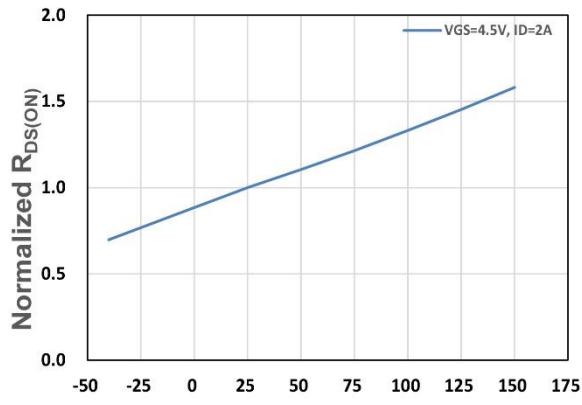
V_{GS} - Gate - Source Voltage (V)

Figure 3. On-Resistance vs. VGS



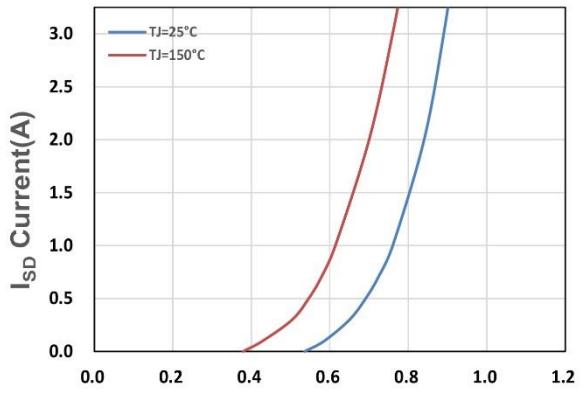
T_j , Junction Temperature(°C)

Figure 4. Gate Threshold Voltage



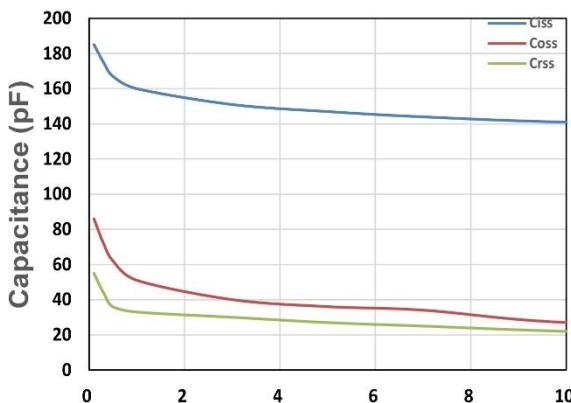
T_j , Junction Temperature(°C)

Figure 5. Drain-Source On Resistance

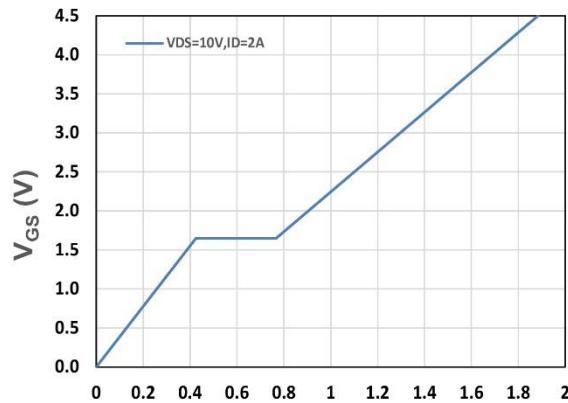


V_{SD} , Source-Drain Voltage(V)

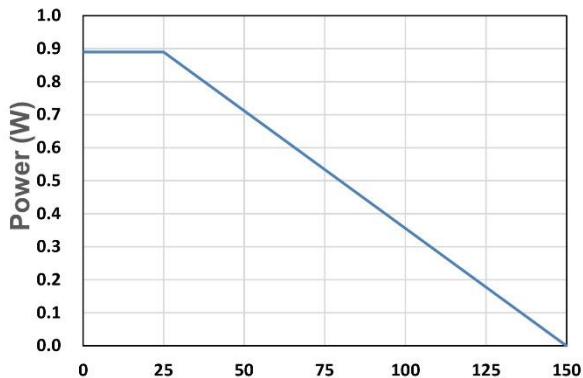
Figure 6. Source-Drain Diode Forward



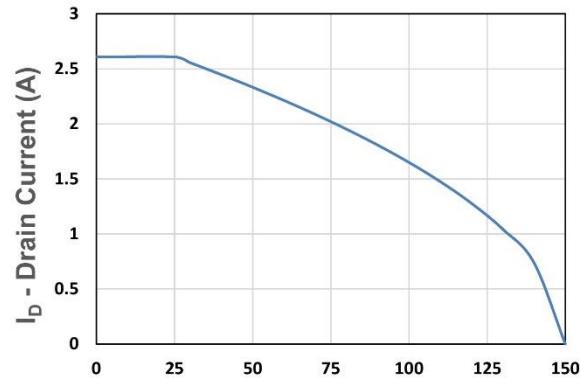
V_{DS} - Drain - Source Voltage (V)
Figure 7. Capacitance



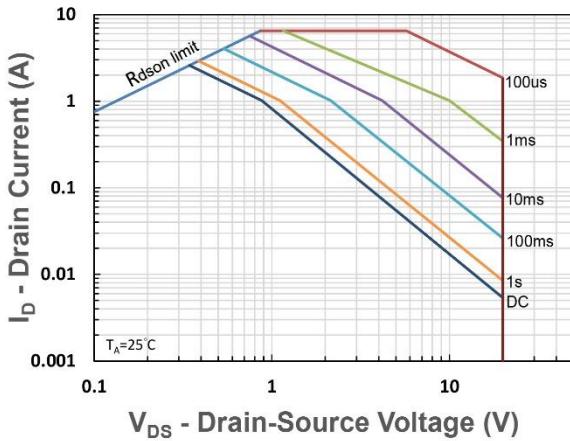
Q_g, Total Gate Charge (nC)
Figure 8. Gate Charge Characteristics



T_A - Ambient Temperature (°C)
Figure 9. Power Dissipation

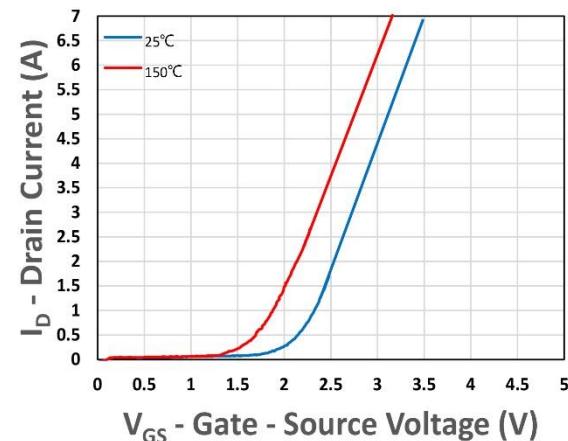


T_A - Ambient Temperature (°C)
Figure 10. Drain Current



V_{DS} - Drain-Source Voltage (V)

Figure 11. Safe Operating Area



V_{GS} - Gate - Source Voltage (V)

Figure 12. Transfer Characteristics

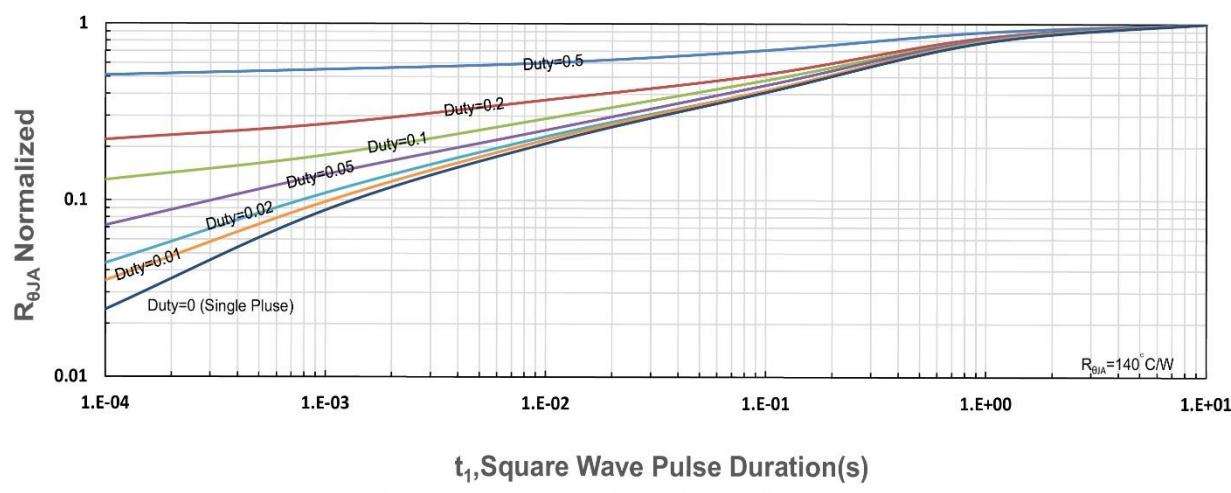


Figure 13. $R_{\theta JA}$ Transient Thermal Impedance