





Power MOSFETS


DATASHEET

LM80034NAK8A

N-Channel
Enhancement Mode MOSFET

 Leadpower-semi CO., LTD.

 sales@leadpower-semi.com

 (03) 6577339 FAX : (03) 6577229

 www.leadpower-semi.com

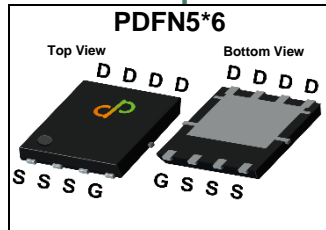


Quality Management Systems

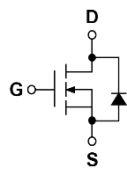
ISO 9001:2015 Certificate

N-Channel Enhancement Mode MOSFET

Pin Description



Symbol



Product Summary

Symbol	N-Channel	Unit
V_{DSS}	80	V
$R_{DS(ON)-Max}$	3.4	m Ω
ID	142	A

Feature

- Fast switching speed
- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- 100% UIS and Rg Tested

Applications

- Power Management in DC/DC Converters
- Server power supply
- Motor control
- Power OR-ing

Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM80034NAK8A	PDFN5*6	Tape & Reel	5000 / Tape & Reel	80034 □□□□□□

Note : □□□□□□ = Lot Code

Absolute Maximum Ratings (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter	N-Channel	Unit	
V_{DSS}	Drain-Source Voltage	80	V	
V_{GSS}	Gate-Source Voltage	±20		
T_J	Maximum Junction Temperature	150	°C	
T_{STG}	Storage Temperature Range	-55 to 150	°C	
I_S	Diode Continuous Forward Current	$T_C=25^\circ C$	38	A
$I_{DM}^{(1)}$	Pulse Drain Current Tested	$T_C=25^\circ C$	370	A
I_D	Continuous Drain Current	$T_C=25^\circ C$	142	A
		$T_C=100^\circ C$	94	
P_D	Maximum Power Dissipation	$T_C=25^\circ C$	125	W
		$T_C=100^\circ C$	50	
I_D	Continuous Drain Current	$T_A=25^\circ C$	21	A
		$T_A=70^\circ C$	17	
P_D	Maximum Power Dissipation	$T_A=25^\circ C$	2.6	W
		$T_A=70^\circ C$	1.7	
$I_{AS}^{(2)}$	Avalanche Current, Single pulse	L=0.1mH	53	A
		L=0.5mH	30	
$E_{AS}^{(2)}$	Avalanche Energy, Single pulse	L=0.1mH	140	mJ
		L=0.5mH	225	

Thermal Characteristics

Symbol	Parameter	Rating	Unit	
$R_{\theta JC}$	Thermal Resistance-Junction to Case	Steady State	1	°C/W
$R_{\theta JA}^{(3)}$	Thermal Resistance-Junction to Ambient	Steady State	48	°C/W

Note ① : Max. current is limited by junction temperature

Note ② : UIS tested and pulse width are limited by maximum junction temperature 150°C

Note ③ : Surface Mounted on 1in² FR-4 board with 1oz

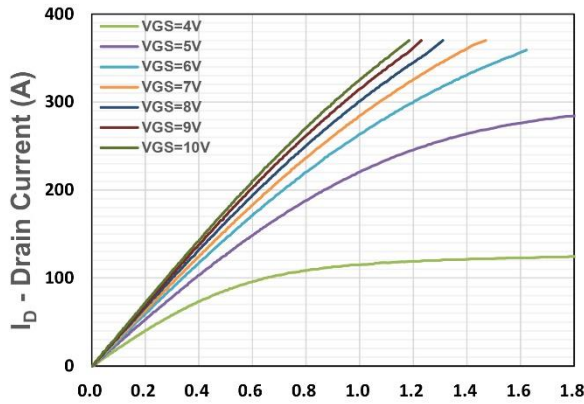
N-Channel Electrical Characteristics (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Electrical Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =250uA	80	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V _{DS} =64V, V _{GS} =0V	-	-	1	uA
V_{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =250uA	1	2	3	V
I_{GSS}	Gate Leakage Current	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
R_{DS(ON)}^④	Drain-Source On-state Resistance	V _{GS} =10V, I _{DS} =20A	-	2.8	3.4	mΩ
		V _{GS} =4.5V, I _{DS} =10A	-	4.1	5.4	
g_{fs}	Forward Transconductance	V _{DS} =5V, I _{DS} =10A	-	37	-	S
Dynamic Characteristics[®]						
R_G	Gate Resistance	V _{GS} =0V, V _{DS} =0V, Freq.=1MHz	-	0.8	-	Ω
C_{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =40V, Freq.=1MHz	-	5075	-	pF
C_{oss}	Output Capacitance					
C_{rss}	Reverse Transfer Capacitance					
t_{d(ON)}	Turn-on Delay Time	V _{GS} =10V, V _{DS} =40V, I _D =40A, R _{GEN} =1Ω	-	15.2	-	nS
t_r	Turn-on Rise Time					
t_{d(OFF)}	Turn-off Delay Time					
t_f	Turn-off Fall Time					
Q_g	Total Gate Charge	V _{GS} =4.5V, V _{DS} =40V, I _D =20A	-	44.6	-	nC
Q_g	Total Gate Charge	V _{GS} =10V, V _{DS} =40V, I _D =20A	-	87.1	-	
Q_{gs}	Gate-Source Charge		-	17.5	-	
Q_{gd}	Gate-Drain Charge		-	18	-	
Source-Drain Characteristics						
V_{SD}^④	Diode Forward Voltage	I _{SD} =10A, V _{GS} =0V	-	0.7	1.1	V
t_{rr}	Reverse Recovery Time	I _F =10A, V _R =64V	-	50.9	-	nS
Q_{rr}	Reverse Recovery Charge	dI _F /dt=100A/μs	-	56.8	-	nC

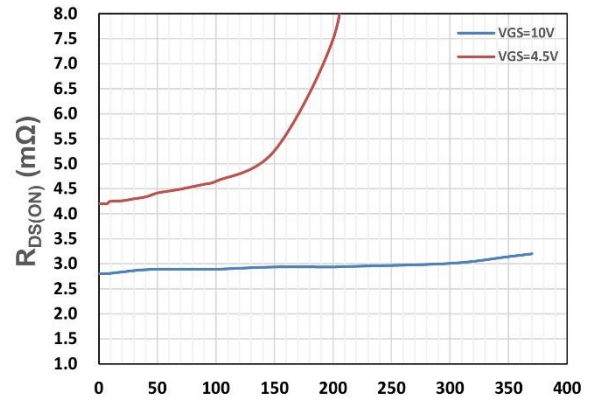
Note ④ : Pulse test (pulse width≤300us, duty cycle≤2%).

Note ⑤ : Guaranteed by design, not subject to production testing.

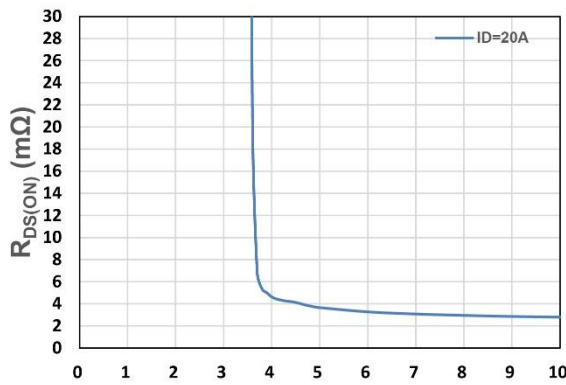
N-Channel Typical Characteristics



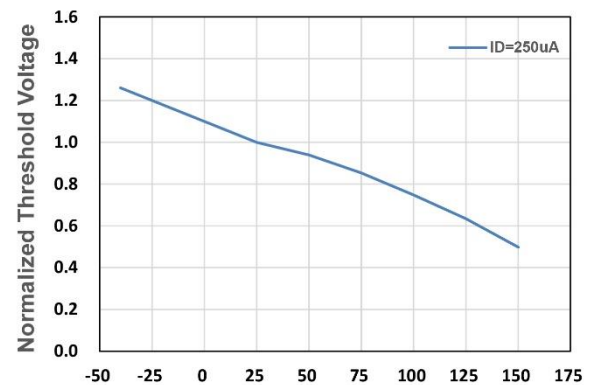
V_{DS} - Drain - Source Voltage (V)
Figure 1. Output Characteristics



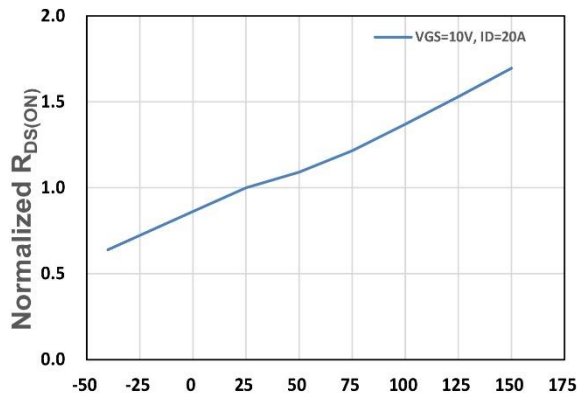
I_D - Drain Current (A)
Figure 2. On-Resistance vs. I_D



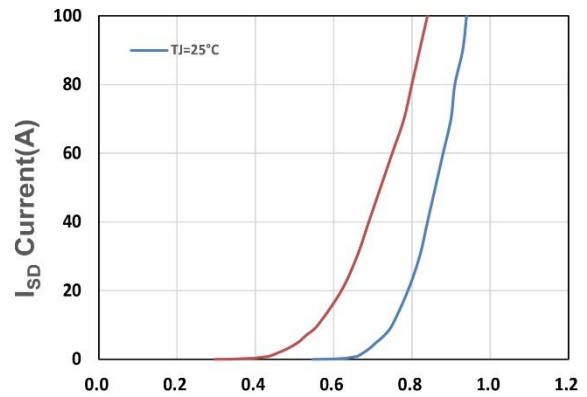
V_{GS} - Gate - Source Voltage (V)
Figure 3. On-Resistance vs. V_{GS}



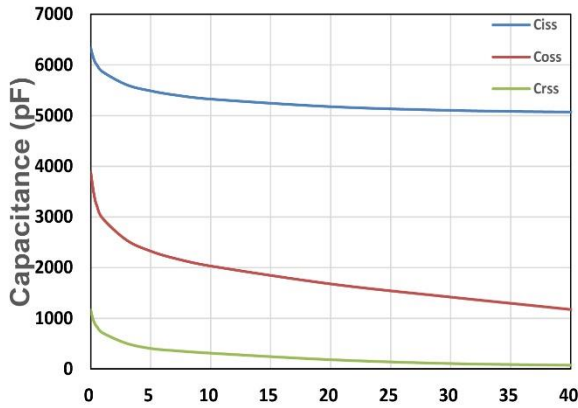
T_j , Junction Temperature($^{\circ}C$)
Figure 4. Gate Threshold Voltage



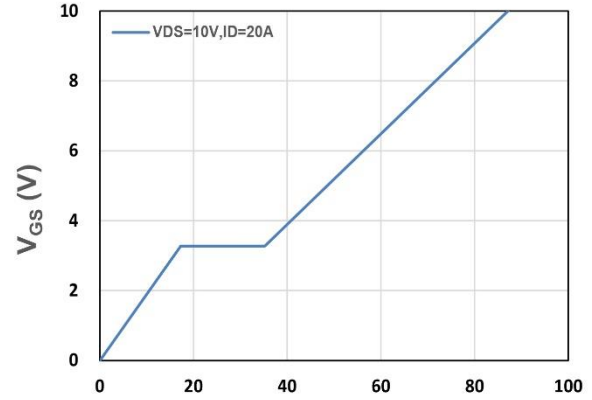
T_j , Junction Temperature($^{\circ}C$)
Figure 5. Drain-Source On Resistance



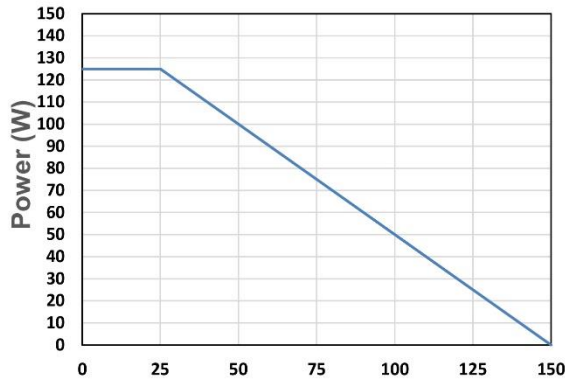
V_{SD} , Source-Drain Voltage(V)
Figure 6. Source-Drain Diode Forward



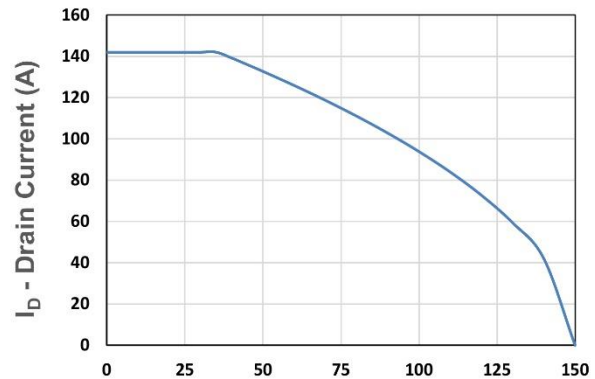
V_{DS} - Drain - Source Voltage (V)
Figure 7. Capacitance



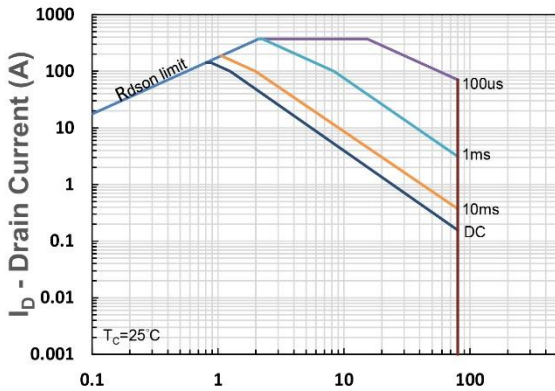
Q_g , Total Gate Charge (nC)
Figure 8. Gate Charge Characteristics



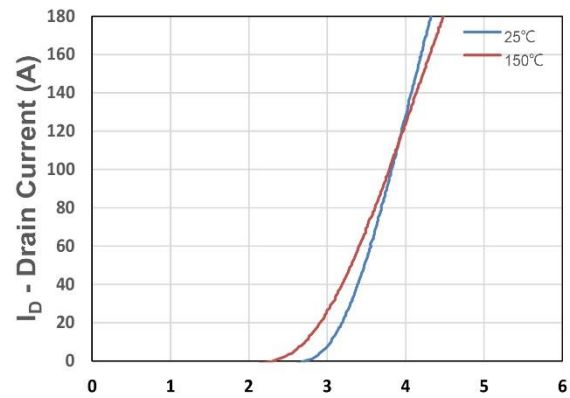
T_c - Case Temperature ($^{\circ}C$)
Figure 9. Power Dissipation



T_c - Case Temperature ($^{\circ}C$)



V_{DS} - Drain-Source Voltage (V)
Figure 11. Safe Operating Area



V_{GS} - Gate - Source Voltage (V)
Figure 12. Transfer Characteristics

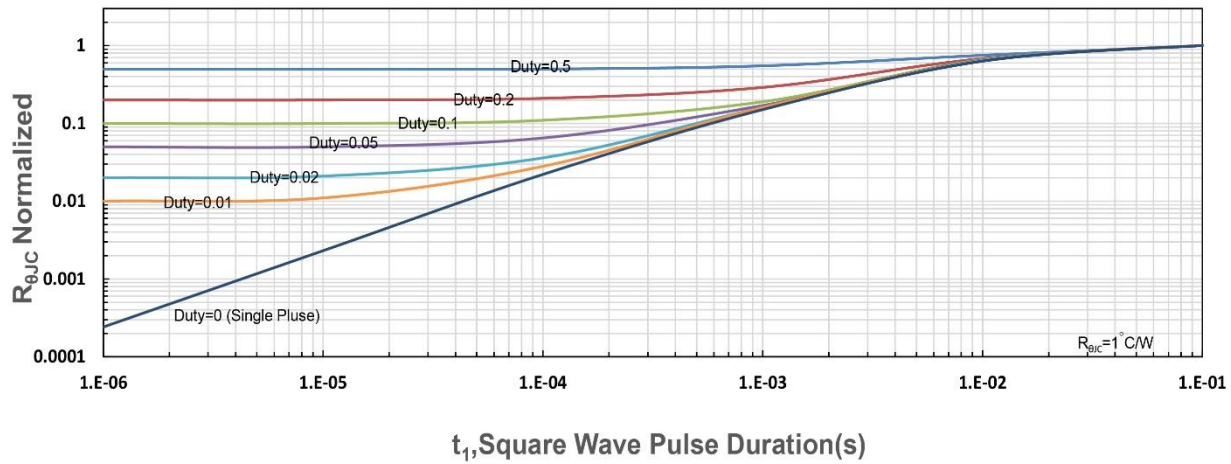


Figure 13. $R_{\theta JC}$ Transient Thermal Impedance