





Power MOSFETS


DATASHEET

LM40018NAM8A

N-Channel
Enhancement Mode MOSFET

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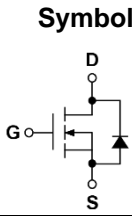
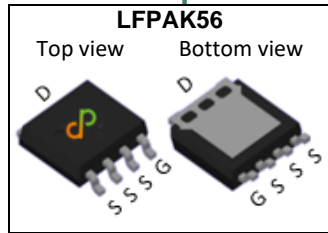


Quality Management Systems

ISO 9001:2015 Certificate

N-Channel Enhancement Mode MOSFET

Pin Description



Product Summary

Symbol	N-Channel	Unit
V_{DSS}	40	V
$R_{DS(ON)-Max}$	2.0	m Ω
I_D	132	A

Feature

- Fast switching speed
- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- 100% UIS and Rg Tested
- Moisture Sensitivity Level MSL1

Applications

- DC-to-DC converters
- Switch Mode Power Supply
- Brushless DC motor control

Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM40018NAM8A	LFPACK56	Tape & Reel	4000 / Tape & Reel	40018 □□□□□□

Note : □□□□□□ = Lot Code

Absolute Maximum Ratings (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter	N-Channel	Unit
V_{DSS}	Drain-Source Voltage	40	V
V_{GSS}	Gate-Source Voltage	±20	
T_J	Maximum Junction Temperature	175	°C
T_{STG}	Storage Temperature Range	-55 to 175	°C
I_S	Diode Continuous Forward Current	$T_C=25^\circ C$ 41	A
I_{SP}	Diode Pulse Current	$T_C=25^\circ C$ 400 ^①	A
I_{DM}	Pulse Drain Current Tested	$T_C=25^\circ C$ 330	A
I_D	Continuous Drain Current	$T_C=25^\circ C$ 132	A
		$T_C=100^\circ C$ 93	
P_D	Maximum Power Dissipation	$T_C=25^\circ C$ 63	W
		$T_C=100^\circ C$ 31	
I_D	Continuous Drain Current	$T_A=25^\circ C$ 29	A
		$T_A=70^\circ C$ 24	
P_D	Maximum Power Dissipation	$T_A=25^\circ C$ 3.0	W
		$T_A=70^\circ C$ 2.1	
$I_{AS}^{②}$	Avalanche Current, Single pulse	L=0.1mH 35	A
		L=0.5mH 18	
$E_{AS}^{②}$	Avalanche Energy, Single pulse	L=0.1mH 61	mJ
		L=0.5mH 81	

Thermal Characteristics

Symbol	Parameter	Rating	Unit
$R_{\theta JC}$	Thermal Resistance-Junction to Case	Steady State	2.4 °C/W
$R_{\theta JA}^{③}$	Thermal Resistance-Junction to Ambient	Steady State	50 °C/W

Note ① : Max. current is limited by bonding

Note ② : UIS tested and pulse width are limited by maximum junction temperature 175°C

Note ③ : Surface Mounted on 1in² FR-4 board with 1oz

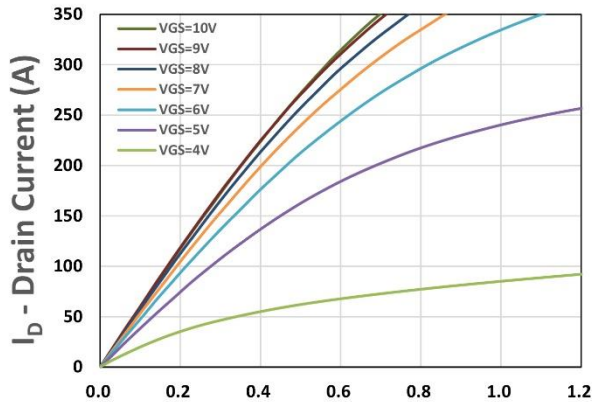
N-Channel Electrical Characteristics (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Electrical Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =250uA	40	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V _{DS} =32V, V _{GS} =0V	-	-	1	uA
V_{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =250uA	1	1.7	2.3	V
I_{GSS}	Gate Leakage Current	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
R_{DS(on)} ^④	Drain-Source On-state Resistance	V _{GS} =10V, I _{DS} =20A	-	1.65	2.0	mΩ
		V _{GS} =4.5V, I _{DS} =15A	-	3.4	4.4	
gfs	Forward Transconductance	V _{DS} =5V, I _{DS} =10A	-	40	-	S
Dynamic Characteristics ^⑥						
R_G	Gate Resistance	V _{GS} =0V, V _{DS} =0V, Freq.=1MHz	-	1.3	-	Ω
C_{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =20V, Freq.=1MHz	-	2303	-	pF
C_{oss}	Output Capacitance					
C_{rss}	Reverse Transfer Capacitance					
td(ON)	Turn-on Delay Time	V _{GS} =10V, V _{DS} =20V, I _D =1A, R _{GEN} =1Ω	-	12	-	nS
t_r	Turn-on Rise Time					
t_{d(OFF)}	Turn-off Delay Time					
t_f	Turn-off Fall Time					
Q_g	Total Gate Charge	V _{GS} =4.5V, V _{DS} =20V, I _D =20A	-	16	-	nC
Q_g	Total Gate Charge	V _{GS} =10V, V _{DS} =20V, I _D =20A	-	33	-	nC
Q_{gs}	Gate-Source Charge					
Q_{gd}	Gate-Drain Charge					
Source-Drain Characteristics						
V_{SD} ^④	Diode Forward Voltage	I _{SD} =25A, V _{GS} =0V	-	0.75	1.1	V
t_{rr}	Reverse Recovery Time	I _F =10A, V _R =20V	-	36	-	nS
Q_{rr}	Reverse Recovery Charge	diF/dt=100A/μs	-	27	-	nC

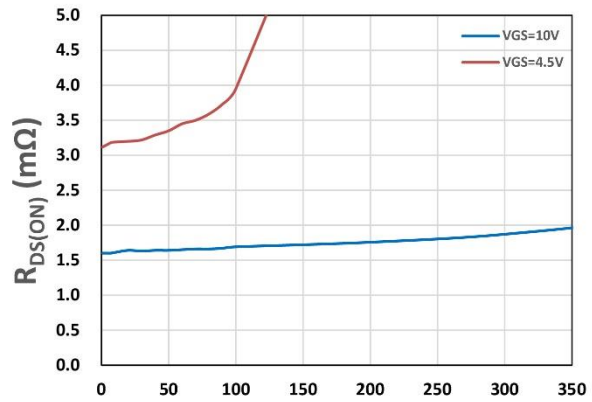
Note ④ : Pulse test (pulse width≤300us, duty cycle≤2%).

Note ⑤ : Guaranteed by design, not subject to production testing.

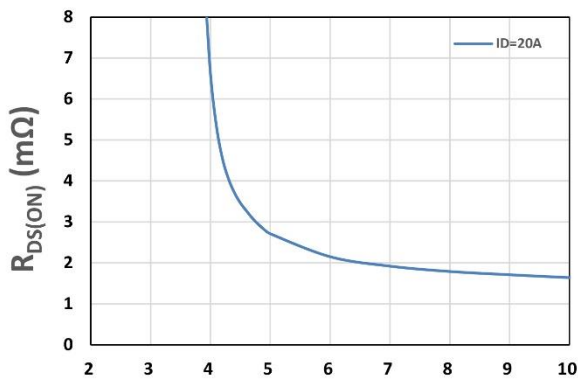
N-Channel Typical Characteristics



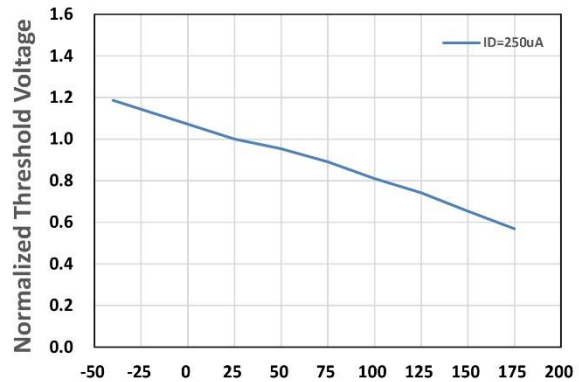
V_{DS} - Drain - Source Voltage (V)
Figure 1. Output Characteristics



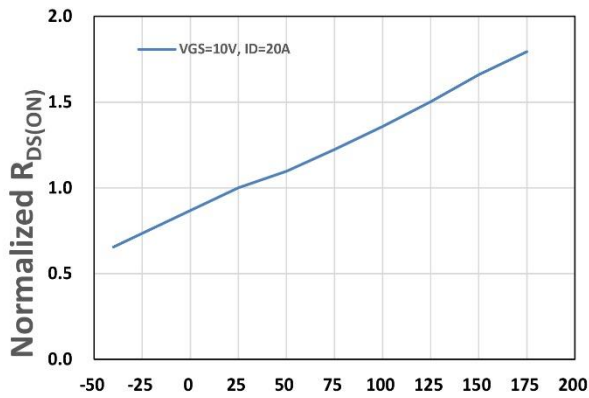
I_D - Drain Current (A)
Figure 2. On-Resistance vs. ID



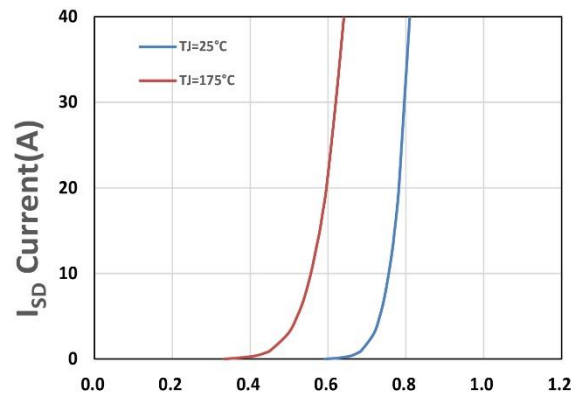
V_{GS} - Gate - Source Voltage (V)
Figure 3. On-Resistance vs. VGS



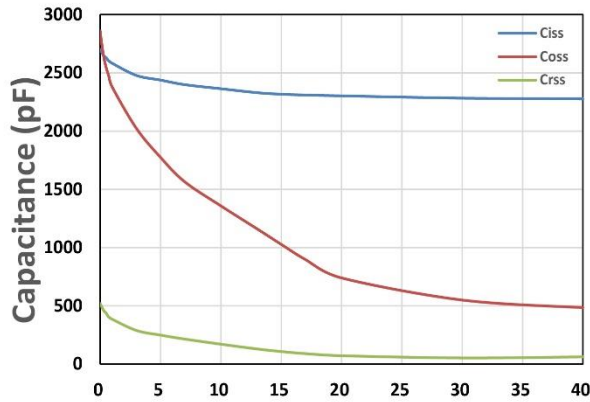
T_j , Junction Temperature($^{\circ}C$)
Figure 4. Gate Threshold Voltage



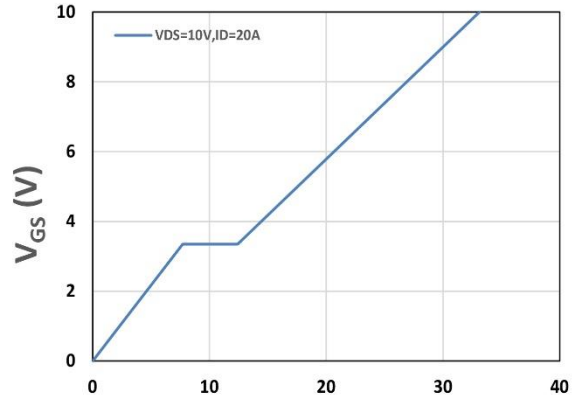
T_j , Junction Temperature($^{\circ}C$)
Figure 5. Drain-Source On Resistance



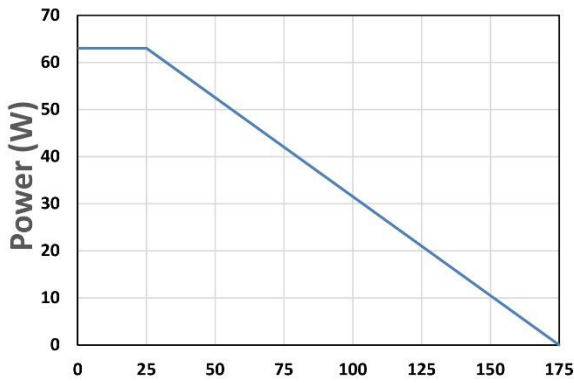
V_{SD} , Source-Drain Voltage(V)
Figure 6. Source-Drain Diode Forward



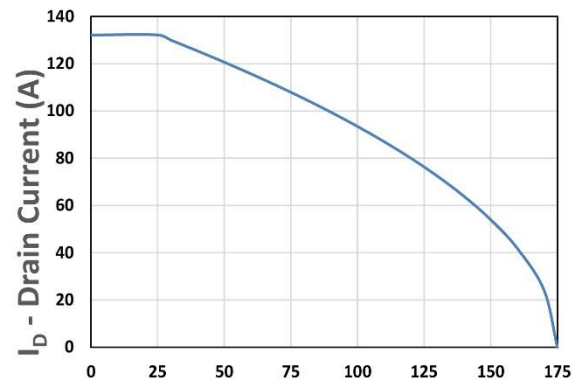
V_{DS} - Drain - Source Voltage (V)
Figure 7. Capacitance



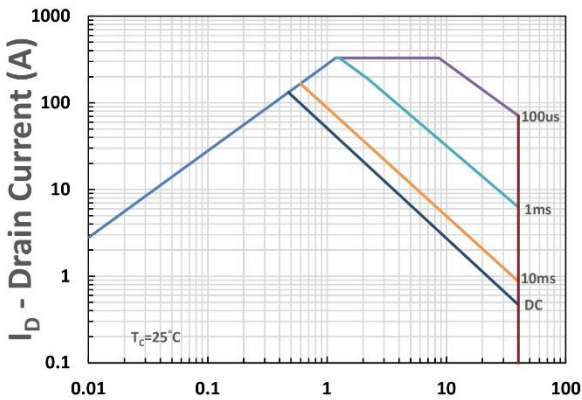
Q_g, Total Gate Charge (nC)
Figure 8. Gate Charge Characteristics



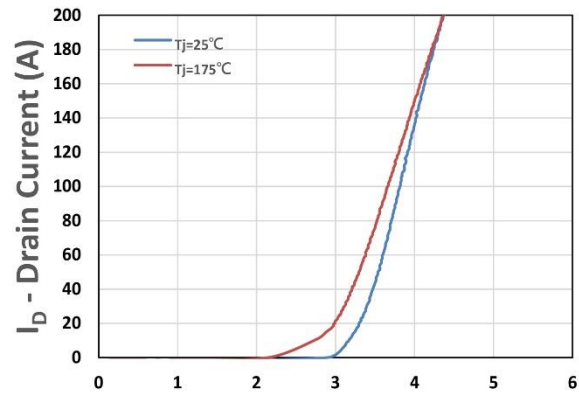
T_C-Case Temperature (°C)
Figure 9. Power Dissipation



T_C-Case Temperature (°C)
Figure 10. Drain Current



V_{DS} - Drain-Source Voltage (V)
Figure 11. Safe Operating Area



V_{GS} - Gate - Source Voltage (V)
Figure 12. Transfer Characteristics

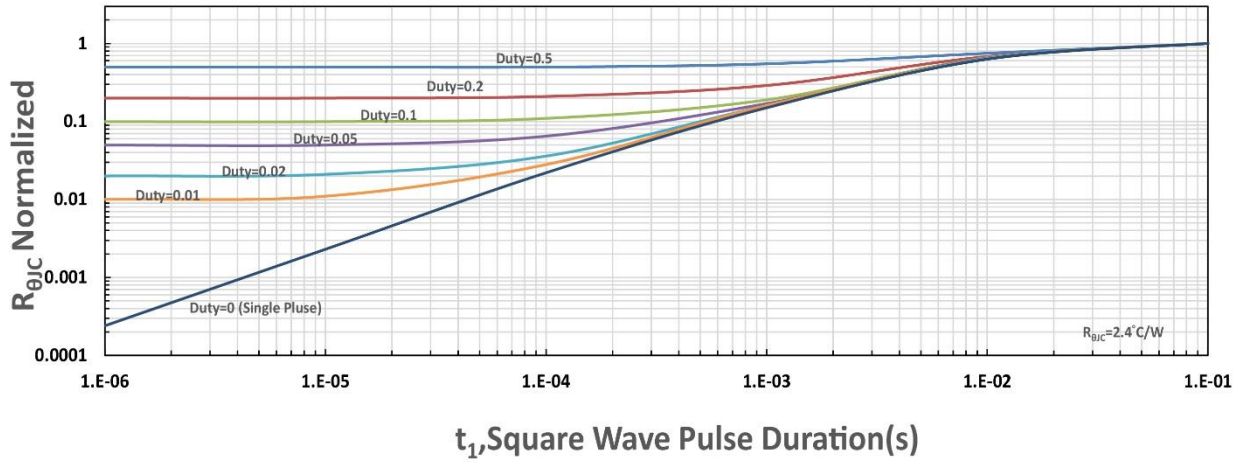


Figure 13. $R_{\theta JC}$ Transient Thermal Impedance