



Power MOSFETS

DATASHEET

LM30210PAK8A

P-Channel
Enhancement Mode MOSFET

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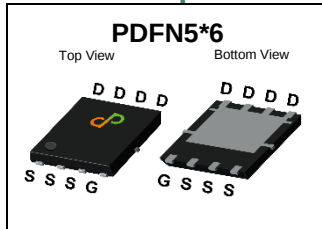


Quality Management Systems

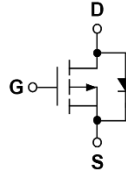
ISO 9001:2015 Certificate

P-Channel Enhancement Mode MOSFET

Pin Description



Symbol



Product Summary

Symbol	P-Channel	Unit
V_{DSS}	-30	V
$R_{DS(ON)-Max}$	23	mΩ
ID	-30	A

Feature

- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- 100% UIS Tested

Applications

- Portable Equipment
- Battery Powered System

Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM30210PAK8A	PDFN5*6	Tape & Reel	5000 / Tape & Reel	30210 □□□□□□

Note : □□□□□□ = Lot Code

Absolute Maximum Ratings ($T_J=25^{\circ}\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	P-Channel	Unit
V_{DSS}	Drain-Source Voltage	-30	V
V_{GSS}	Gate-Source Voltage	±25	
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-55 to 150	°C
$I_{DM}^{①}$	Pulse Drain Current Tested	$T_c=25^{\circ}\text{C}$	A
I_D	Continuous Drain Current	$T_c=25^{\circ}\text{C}$	A
		$T_c=100^{\circ}\text{C}$	
P_D	Maximum Power Dissipation	$T_c=25^{\circ}\text{C}$	W
		$T_c=100^{\circ}\text{C}$	
$I_{AS}^{②}$	Avalanche Current, Single pulse	$L=0.1\text{mH}$	A
$E_{AS}^{②}$	Avalanche Energy, Single pulse	$L=0.1\text{mH}$	mJ

Thermal Characteristics

Symbol	Parameter	Rating	Unit
$R_{\theta JC}$	Thermal Resistance-Junction to Case	Steady State	3.9
$R_{\theta JA}^{③}$	Thermal Resistance-Junction to Ambient	Steady State	75

Note ① : Max. current is limited by bonding wire

Note ② : UIS tested and pulse width are limited by maximum junction temperature 150°C

Note ③ : Surface Mounted on 1in^2 FR-4 board with 1oz.

P-Channel Electrical Characteristics ($T_J=25^{\circ}\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Electrical Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =-250uA	-30	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-24V, V _{GS} =0V	-	-	-1	uA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =-250uA	-1	-1.7	-2.3	V
I _{GSS}	Gate Leakage Current1	V _{GS} =±25V, V _{DS} =0V	-	-	±100	nA
R _{DS(ON)} ④	Drain-Source On-state Resistance	V _{GS} =-10V, I _{DS} =-15A	-	19	23	mΩ
		V _{GS} =-4.5V, I _{DS} =-10A	-	26	34	
gfs	Forward Transconductance	V _{DS} =-5V, I _{DS} =-7.5A	-	14	-	S
Dynamic Characteristics ⑥						
R _G	Gate Resistance	V _{GS} =0V,V _{DS} =0V, Freq.=1MHz	-	15	-	Ω
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-15V, Freq.=1MHz	-	1223	-	pF
C _{oss}	Output Capacitance		-	135	-	
C _{rss}	Reverse Transfer Capacitance		-	116	-	
td(ON)	Turn-on Delay Time	V _{GS} =-10V,V _{DS} =-15V, I _D =-1A,R _{GEN} =6Ω	-	3.2	-	nS
t _r	Turn-on Rise Time		-	22.8	-	
t _{d(OFF)}	Turn-off Delay Time		-	105.2	-	
t _f	Turn-off Fall Time		-	47.8	-	
Q _g	Total Gate Charge	V _{GS} =-4.5V,V _{DS} =-15V I _D =-15A	-	13.3	-	nC
Q _g	Total Gate Charge	V _{GS} =-10V,V _{DS} =-15V, I _D =-15A	-	27.3	-	
Q _{gs}	Gate-Source Charge		-	5.19	-	
Q _{gd}	Gate-Drain Charge		-	5.32	-	
Source-Drain Characteristics						
V _{SD} ④	Diode Forward Voltage	I _{SD} =-7.5A, V _{GS} =0V	-	-0.8	-1.1	V
t _{rr}	Reverse Recovery Time	I _F =-7.5A, V _R =-15V	-	12.7	-	nS
Q _{rr}	Reverse Recovery Charge	dI _F /dt=100A/μs	-	5.5	-	nC

Note ④ : Pulse test (pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$).

Note ⑤ : Guaranteed by design, not subject to production testing.

P-Channel Typical Characteristics

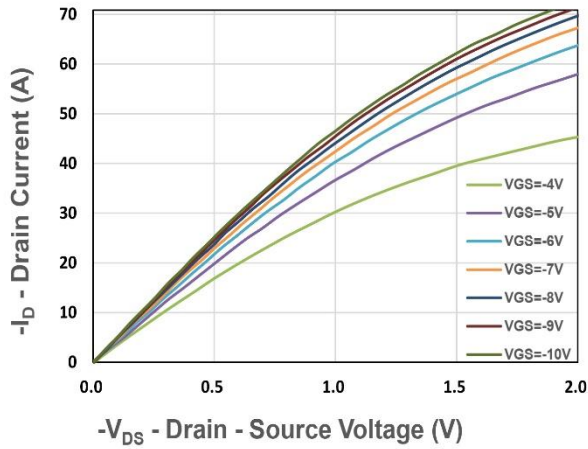


Figure 1. Output Characteristics

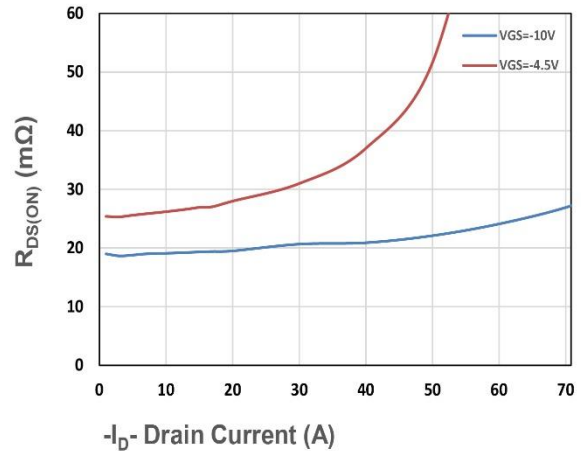


Figure 2. On-Resistance vs. ID

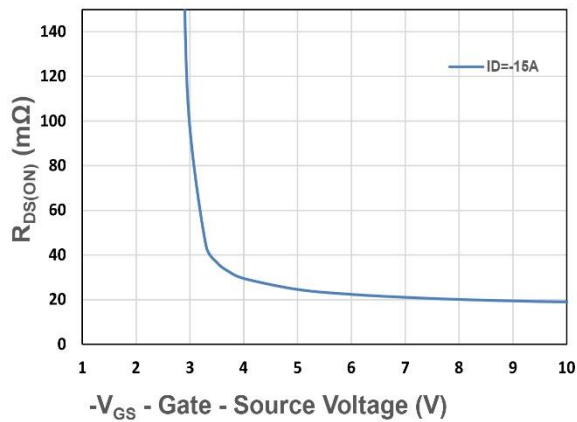


Figure 3. On-Resistance vs. VGS

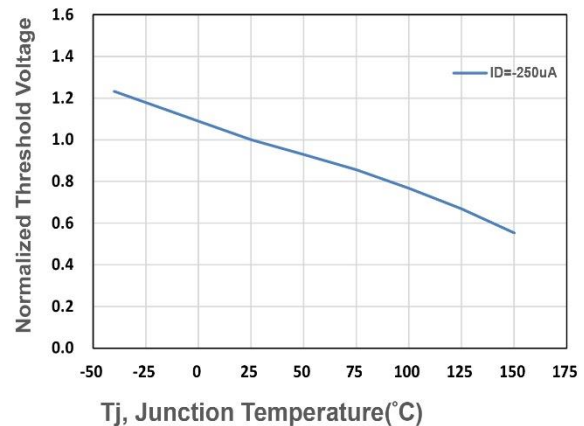


Figure 4. Gate Threshold Voltage

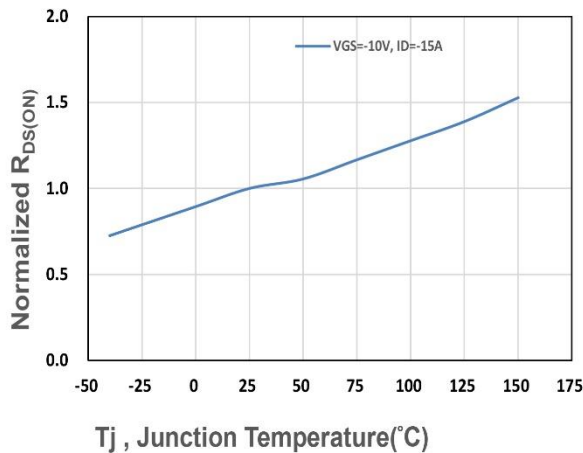


Figure 5. Drain-Source On Resistance

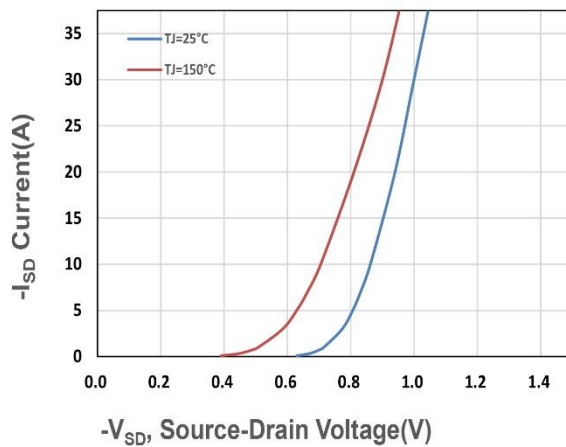


Figure 6. Source-Drain Diode Forward

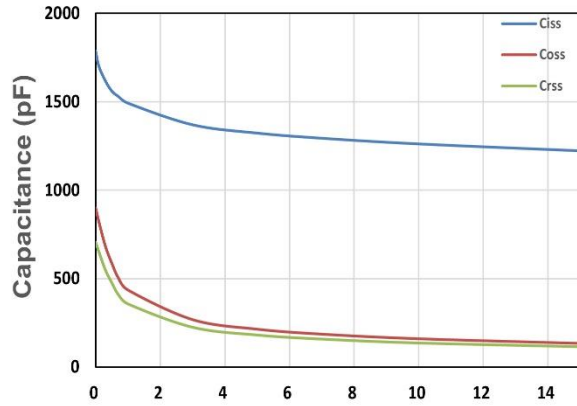


Figure 7. Capacitance

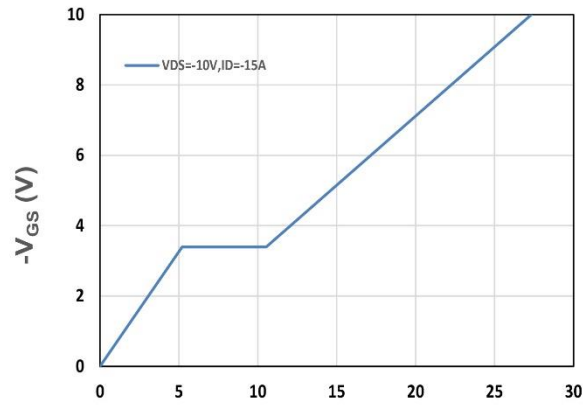


Figure 8. Gate Charge Characteristics

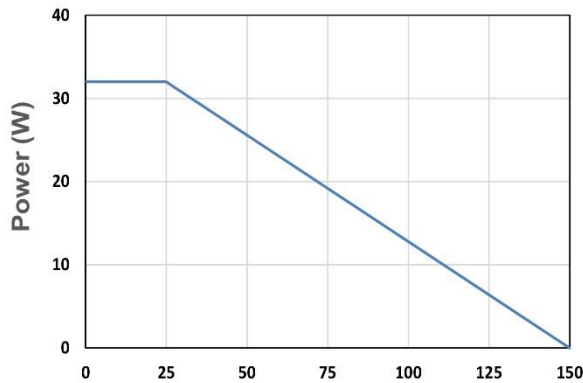


Figure 9. Power Dissipation

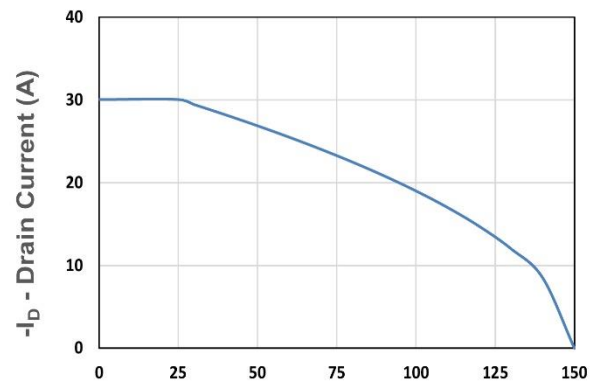


Figure 10. Drain Current

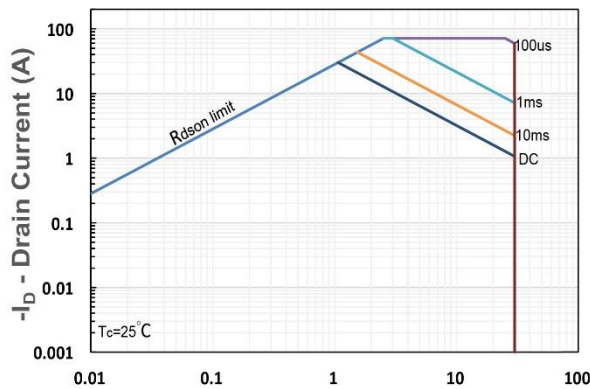


Figure 11. Safe Operating Area

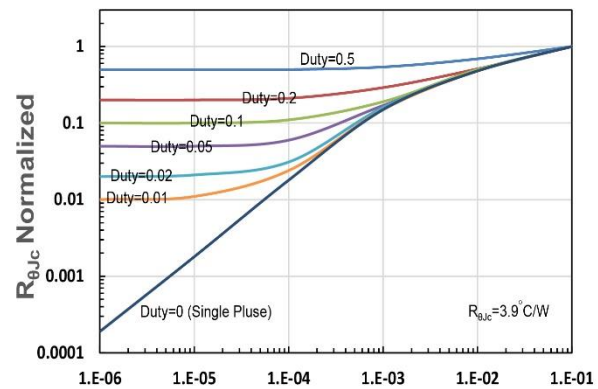


Figure 12. $R_{\theta JC}$ Transient Thermal Impedance