# Power MOSFETS

## DATASHEET

## LM138NEI3A

N-Channel

Enhancement Mode MOSFET

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Quality Management Systems

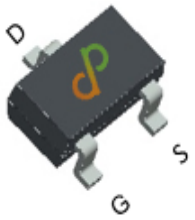
ISO 9001:2015 Certificate

# LM138NEI3A

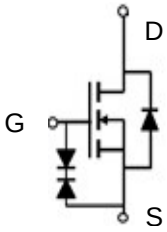
## N-Channel Enhancement Mode MOSFET

### Pin Description

SOT-23 (TOP view)




Symbol




### Ordering Information

| Symbol | N-Channel | Unit |
|---|---|---|
| $V_{DSS}$ | **50** | **V** |
| $R_{DS(ON)-Max}$ | **1.9** | **Ω** |
| $I_D$ | **0.31** | **A** |

### Feature

- Low Vth low gate drive
- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- ESD protection

### Applications

- Small signal application
- Load switch

### Ordering Information

| Orderable Part Number | Package Type | Form | Shipping | Marking |
|---|---|---|---|---|
| LM138NEI3A | SOT-23 | Tape & Reel | 3000 / Tape & Reel | 16□□□ |

### Absolute Maximum Ratings ($T_J$=25°C Unless Otherwise Noted)

| Symbol | Parameter | | N-Channel | Unit |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 50 | V |
| $V_{GSS}$ | Gate-Source Voltage | | ±20 | |
| $T_J$ | Maximum Junction Temperature | | 150 | °C |
| $T_{STG}$ | Storage Temperature Range | | -55 to 150 | °C |
| $I_{DM}$① | Pulse Drain Current Tested | $T_A$=25°C | 0.77 | A |
| $I_D$ | Continuous Drain Current | $T_A$=25°C | 0.31 | A |
| | | $T_A$=70°C | 0.25 | |
| $P_D$ | Maximum Power Dissipation | $T_A$=25°C | 0.36 | W |
| | | $T_A$=70°C | 0.23 | |

### Thermal Characteristics

| Symbol | Parameter | | Rating | Unit |
|---|---|---|---|---|
| $R_{\theta JA}$② | Thermal Resistance-Junction to Ambient | Steady State | 350 | °C/W |

Note ①：Max. current is limited by junction temperature.
Note ②：Surface Mounted on 1in$^2$ FR-4 board with 1oz.

## N-Channel Electrical Characteristics ($T_J$=25°C Unless Otherwise Noted)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Static Electrical Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$=0V, $I_{DS}$=250uA | 50 | - | - | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$=40V, $V_{GS}$=0V | - | - | 1 | uA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$, $I_{DS}$=250uA | 0.6 | 1.2 | 1.5 | V |
| $I_{GSS}$ | Gate Leakage Current | $V_{GS}$=±20V, $V_{DS}$=0V | - | - | ±10 | uA |
| $R_{DS(ON)}$③ | Drain-Source On-state Resistance | $V_{GS}$=10V, $I_{DS}$=0.23A | - | 1.6 | 1.9 | Ω |
| | | $V_{GS}$=4.5V, $I_{DS}$=0.19A | | 1.7 | 2.2 | |
| | | $V_{GS}$=2.5V, $I_{DS}$=0.05A | - | 2 | - | |
| gfs | Forward Transconductance | $V_{DS}$=2V, $I_{DS}$=0.18A | - | 0.6 | - | S |
| **Dynamic Characteristics** ④ | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{GS}$=0V, $V_{DS}$=30V, Freq.=1MHz | - | 25.2 | - | pF |
| $C_{oss}$ | Output Capacitance | | - | 3.2 | - | |
| $C_{rss}$ | Reverse Transfer Capacitance | | - | 2.1 | - | |
| $td_{(ON)}$ | Turn-on Delay Time | $V_{GS}$=10V,$V_{DS}$=50V, $I_D$=0.23A,$R_{GEN}$=10Ω | - | 0.5 | - | nS |
| $t_r$ | Turn-on Rise Time | | - | 19.4 | - | |
| $t_{d(OFF)}$ | Turn-off Delay Time | | - | 26.2 | - | |
| $t_f$ | Turn-off Fall Time | | - | 22.4 | - | |
| $Q_g$ | Total Gate Charge | $V_{GS}$=4.5V,$V_{DS}$=50V $I_D$=1A | - | 0.9 | - | nC |
| $Q_g$ | Total Gate Charge | $V_{GS}$=10V,$V_{DS}$=50V, $I_D$=1A | - | 1.7 | - | |
| Qgs | Gate-Source Charge | | - | 0.3 | - | |
| Qgd | Gate-Drain Charge | | - | 0.3 | - | |
| **Source-Drain Characteristics** | | | | | | |
| $V_{SD}$③ | Diode Forward Voltage | $I_{SD}$=0.23A, $V_{GS}$=0V | - | 0.8 | 1.1 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_F$=0.5A, $V_{GS}$=0 $dI_F/dt$=100A/μs | - | 7.2 | - | nS |
| $Q_{rr}$ | Reverse Recovery Charge | | - | 1.9 | - | nC |

Note ③：Pulse test (pulse width≤300us, duty cycle≤2%).
Note ④：Guaranteed by design, not subject to production testing.

## N-Channel Typical Characteristics

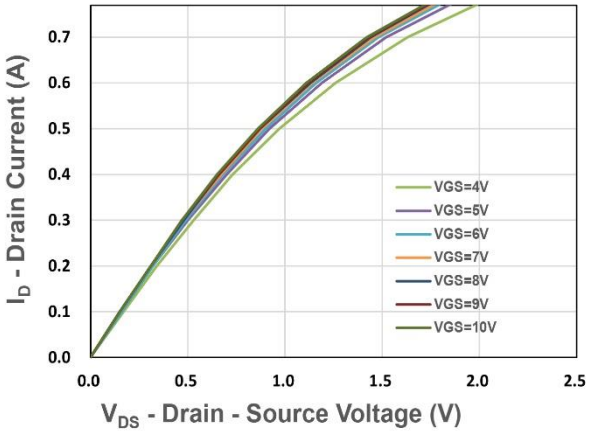



Figure 1. Output Characteristics

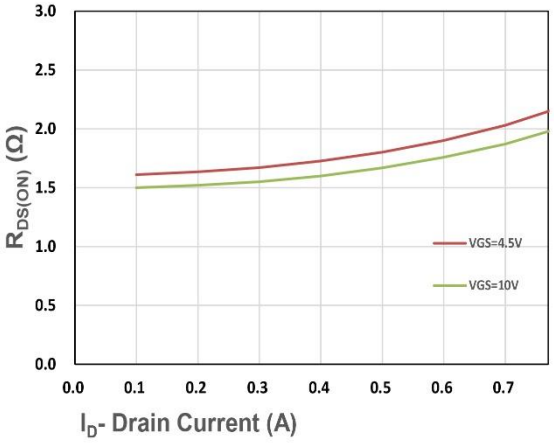



Figure 2. On-Resistance vs. ID

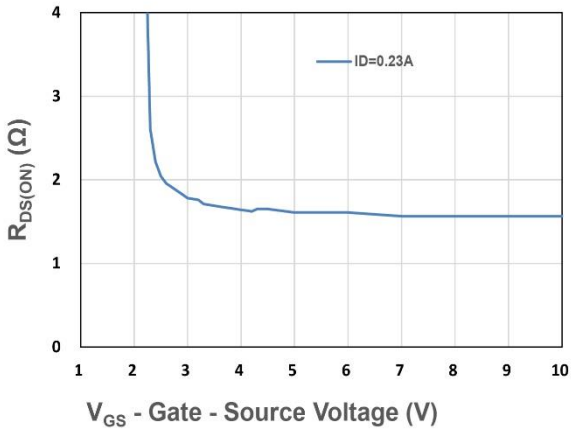



Figure 3. On-Resistance vs. VGS

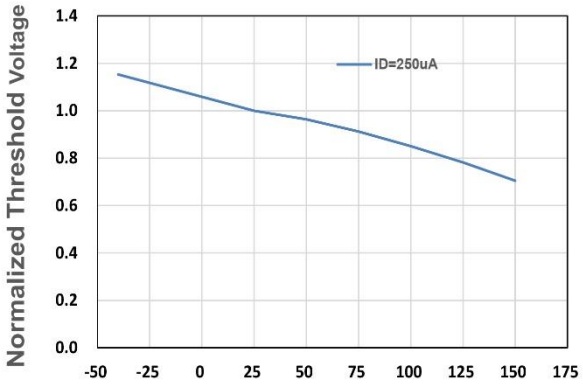



Figure 4. Gate Threshold Voltage

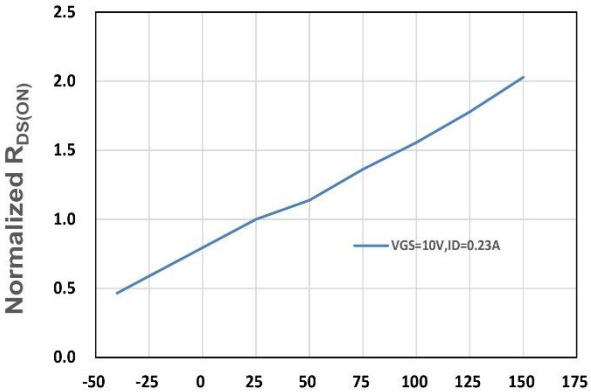



Figure 5. Drain-Source On Resistance

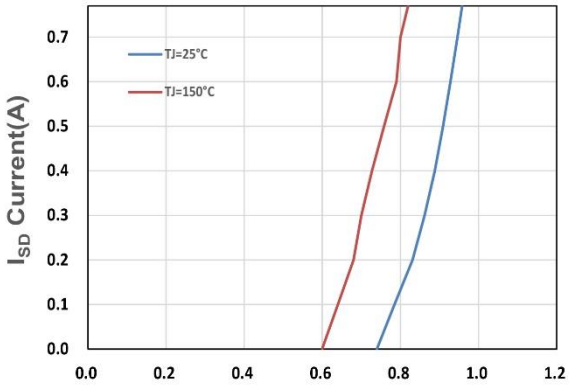



Figure 6. Source-Drain Diode Forward

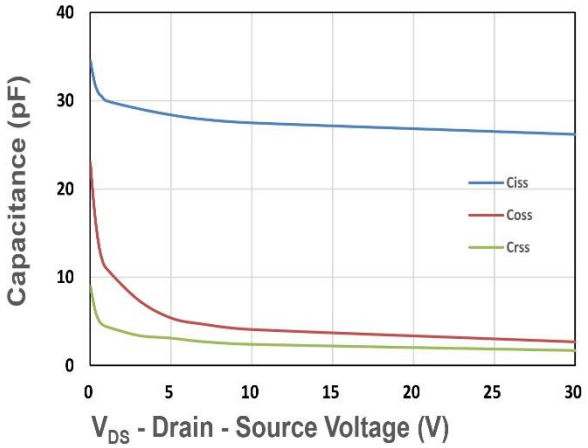



Figure 7. Capacitance

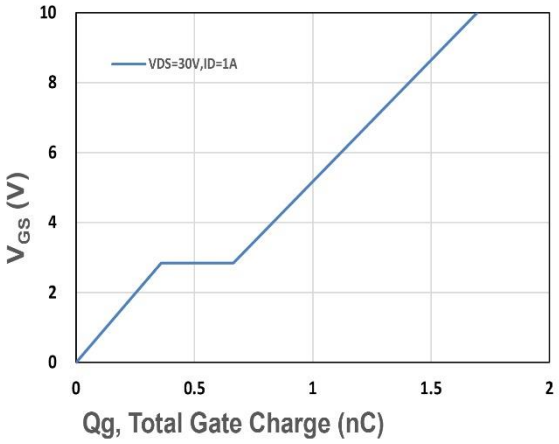



Figure 8. Gate Charge Characteristics

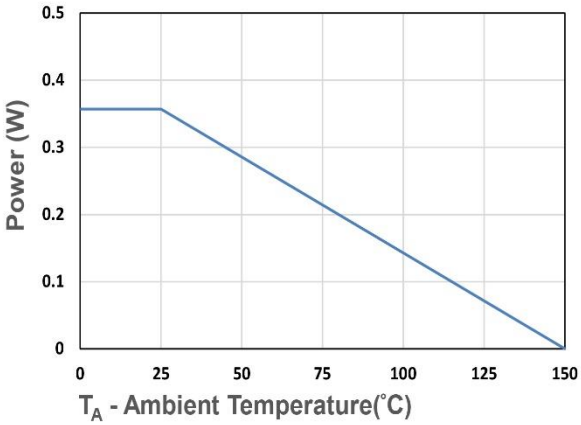



Figure 9. Power Dissipation

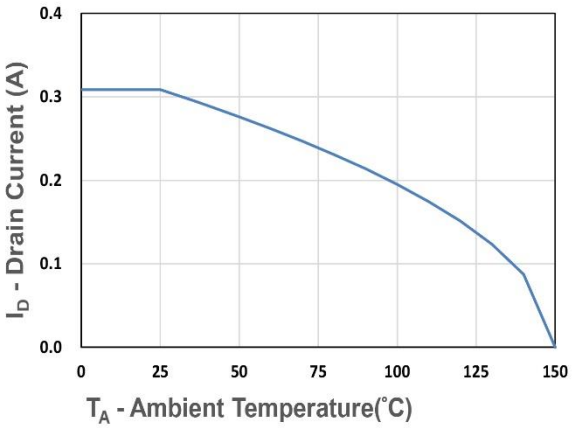



Figure 10. Drain Current

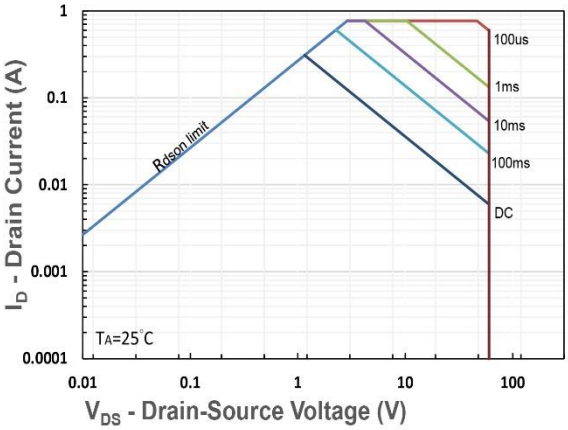



Figure 11. Safe Operating Area

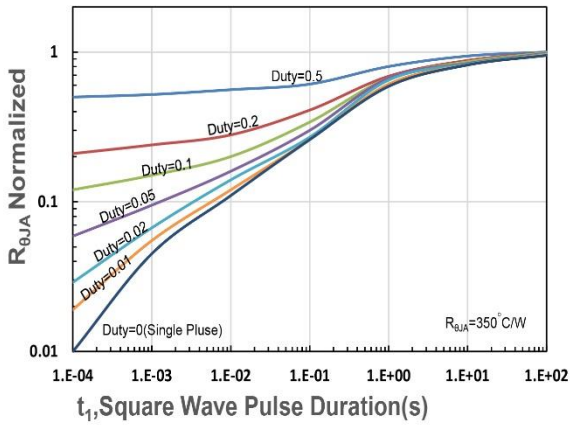



Figure 12. RθJA Transient Thermal Impedance