



Power MOSFETS

DATASHEET

LM1A043NHV2A

N-Channel
Enhancement Mode MOSFET

- Leadpower-semiconductor Corp., Ltd
- sales@leadpower-semi.com
- (03) 6577339 FAX : (03) 6577229
- www.leadpower-semi.com



Quality Management Systems
ISO 9001:2015 Certificate

N-Channel Enhancement Mode MOSFET

Pin Description

TO-263-2L (TOP view)	Symbol	Symbol	N-Channel	Unit	
			V _{DSS}	100	V
			R _{DS(ON)-Max}	4.6	mΩ
			I _D	122	A

Feature

- High Speed Power Switching
- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- 100% UIS Tested

Product Summary

Applications

- Synchronous Rectification in SMPS
- Hard Switching and High Speed Circuit

Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM1A043NHV2A	TO-263-2L	Tape & Reel	800 / Reel	1A043 □□□□□□

Note : □□□□□□ = Lot Code

Absolute Maximum Ratings (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter	N-Channel	Unit
V _{DSS}	Drain-Source Voltage	100	V
V _{GSS}	Gate-Source Voltage	±20	
T _J	Maximum Junction Temperature	150	°C
T _{TSG}	Storage Temperature Range	-55 to 150	°C
I _S	Diode Continuous Forward Current	T _c =25°C 175	A
I _{DM}	Pulse Drain Current Tested	T _c =25°C 380	A
I _D	Continuous Drain Current	T _c =25°C 122 ^①	A
		T _c =100°C 122 ^①	
P _D	Maximum Power Dissipation	T _c =25°C 192	W
		T _c =100°C 77	
I _D	Continuous Drain Current	T _A =25°C 21	A
		T _A =70°C 16.7	
P _D	Maximum Power Dissipation	T _A =25°C 2.0	W
		T _A =70°C 1.3	
I _{AS^②}	Avalanche Current, Single pulse	L=0.1mH 56	A
		L=0.5mH 30	
E _{AS^②}	Avalanche Energy, Single pulse	L=0.1mH 156	mJ
		L=0.5mH 225	

Thermal Characteristics

Symbol	Parameter	Rating	Unit
R _{θJC}	Thermal Resistance-Junction to Case	Steady State 0.65	°C/W
R _{θJA^③}	Thermal Resistance-Junction to Ambient	Steady State 62	°C/W

Note ① : Max. current is limited by bonding wire

Note ② : UIS tested and pulse width are limited by maximum junction temperature 150°C

Note ③ : Surface Mounted on 1in² FR-4 board with 1oz.

N-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Electrical Characteristics						
$\mathbf{BV_{DSS}}$	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$, $I_{DS}=250\mu\text{A}$	100	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=80\text{V}$, $V_{GS}=0\text{V}$	-	-	1	μA
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_{DS}=250\mu\text{A}$	2	3	4	V
I_{GSS}	Gate Leakage Current	$V_{GS}=\pm 20\text{V}$, $V_{DS}=0\text{V}$	-	-	± 100	nA
$R_{DS(\text{ON})}^{\circledast}$	Drain-Source On-state Resistance	$V_{GS}=10\text{V}$, $I_{DS}=20\text{A}$	-	3.9	4.6	$\text{m}\Omega$
g_{fs}	Forward Transconductance	$V_{DS}=5\text{V}$, $I_{DS}=10\text{A}$	-	4.18	-	S
Dynamic Characteristics ^⑤						
R_G	Gate Resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, Freq.=1MHz	-	0.54	-	Ω
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=50\text{V}$, Freq.=1MHz	-	4176	-	pF
C_{oss}	Output Capacitance		-	1190	-	
C_{rss}	Reverse Transfer Capacitance		-	36	-	
$t_{d(\text{ON})}$	Turn-on Delay Time	$V_{GS}=10\text{V}$, $V_{DS}=25\text{V}$, $I_D=1\text{A}$, $R_{GEN}=3\Omega$	-	12.85	-	nS
t_r	Turn-on Rise Time		-	6.35	-	
$t_{d(\text{OFF})}$	Turn-off Delay Time		-	34.9	-	
t_f	Turn-off Fall Time		-	65.55	-	
Q_g	Total Gate Charge	$V_{GS}=10\text{V}$, $V_{DS}=50\text{V}$, $I_D=20\text{A}$	-	72.7	-	nC
Q_{gs}	Gate-Source Charge		-	21.6	-	
Q_{gd}	Gate-Drain Charge		-	20.7	-	
Source-Drain Characteristics						
V_{SD}^{\circledast}	Diode Forward Voltage	$I_{SD}=10\text{A}$, $V_{GS}=0\text{V}$	-	0.75	1.1	V
t_{rr}	Reverse Recovery Time	$I_F=10\text{A}$, $V_R=50\text{V}$	-	40.4	-	nS
Q_{rr}	Reverse Recovery Charge	$dI_F/dt=100\text{A}/\mu\text{s}$	-	80.15	-	nC

Note ④ : Pulse test (pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$).

Note ⑤ : Guaranteed by design, not subject to production testing.

N-Channel Typical Characteristics

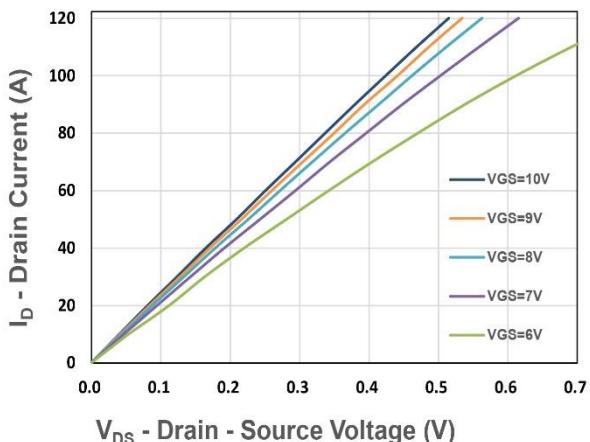


Figure 1. Output Characteristics

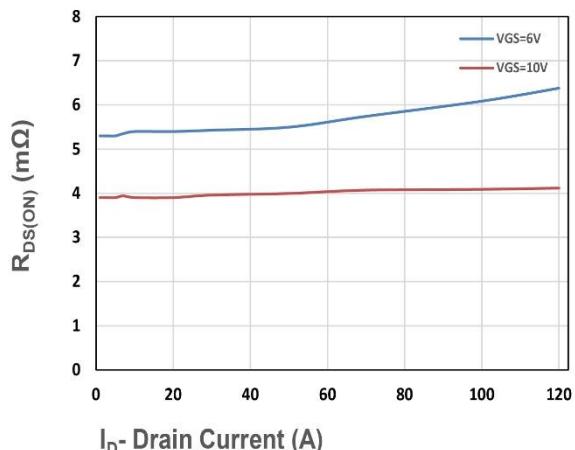


Figure 2. On-Resistance vs. ID

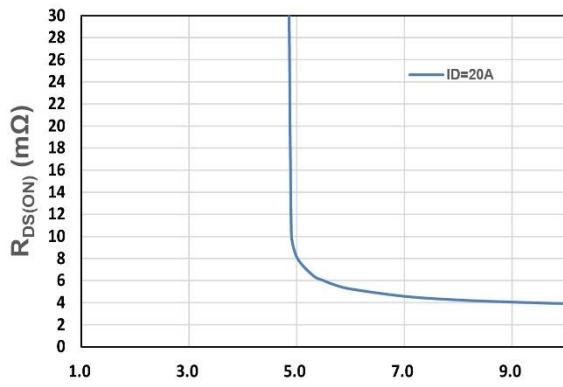


Figure 3. On-Resistance vs. VGS

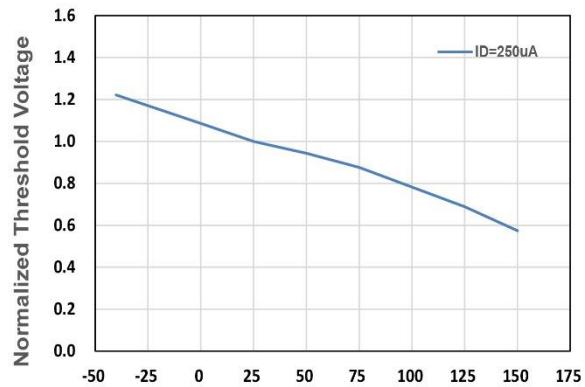


Figure 4. Gate Threshold Voltage

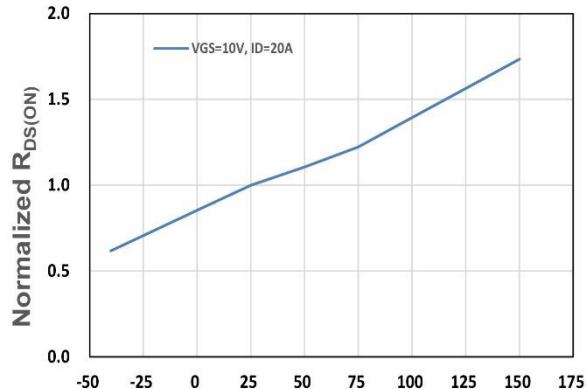


Figure 5. Drain-Source On Resistance

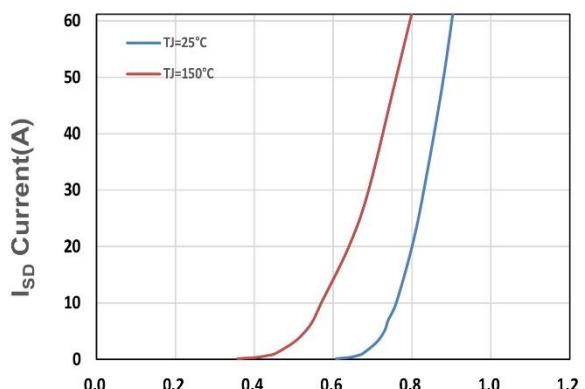


Figure 6. Source-Drain Diode Forward

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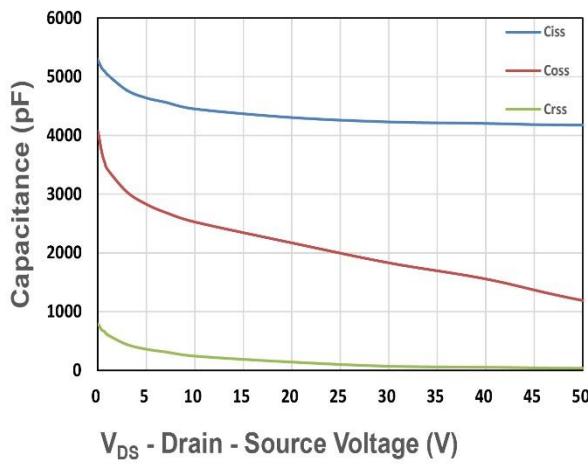


Figure 7. Capacitance

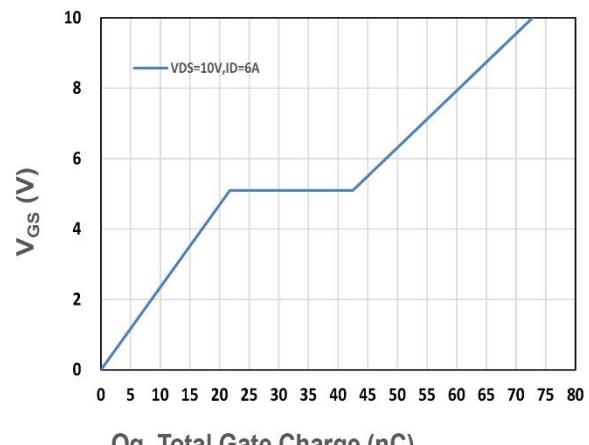


Figure 8. Gate Charge Characteristics

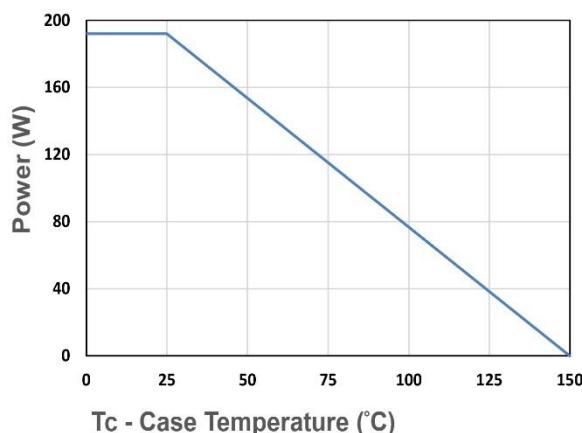


Figure 9. Power Dissipation

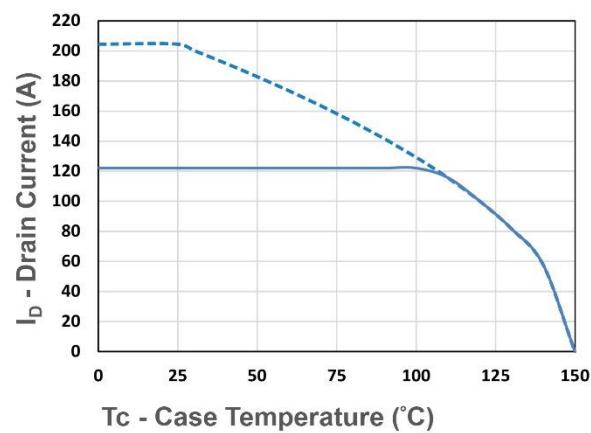


Figure 10. Drain Current

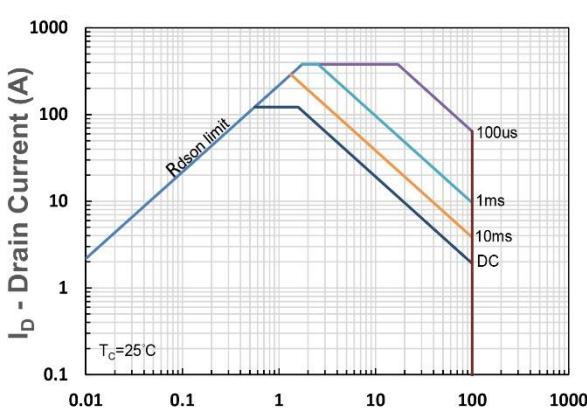


Figure 11. Safe Operating Area

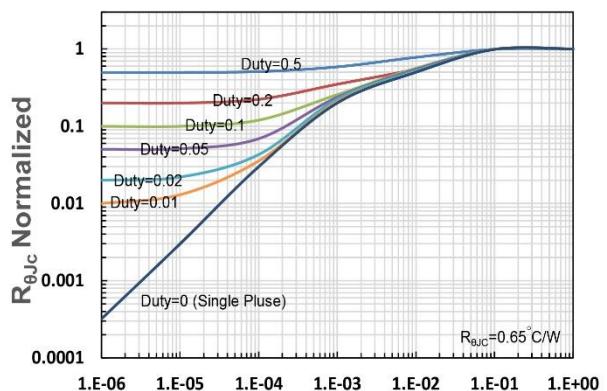


Figure 12. $R_{θJC}$ Transient Thermal Impedance