Power MOSFETS

DATASHEET

LM1AA00NAO2A

N-Channel

Enhancement Mode MOSFET

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Quality Management Systems

ISO 9001:2015 Certificate

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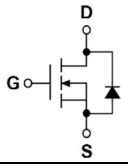
Pin Description

TO-252-2L	Symbol
	

Product Summary

Symbol	N-Channel	Unit
V_{DSS}	100	V
$R_{DS(ON)}$-Max	100	mΩ
ID	19.2	A

Feature

- Optimize factor of Rdson and Qg
- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- 100% UIS Tested

Applications

- DC-DC Conversion
- Networking Switch

Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM1AA00NAO2A	TO-252-2L	Tape & Reel	3000 / Tape & Reel	1AA00 □□□□□□

Note：□□□□□□ = Lot Code

Absolute Maximum Ratings (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter		N-Channel	Unit
V_{DSS}	Drain-Source Voltage		100	V
V_{GSS}	Gate-Source Voltage		±20	
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature Range		-55 to 150	°C
I_S	Diode Continuous Forward Current	T_C=25°C	33	A
I_{DM}①	Pulse Drain Current Tested	T_C=25°C	48	A
I_D	Continuous Drain Current	T_C=25°C	19.2	A
		T_C=100°C	12.1	
P_D	Maximum Power Dissipation	T_C=25°C	36.8	W
		T_C=100°C	14.7	
I_D	Continuous Drain Current	T_A=25°C	4.6	A
		T_A=70°C	3.7	
P_D	Maximum Power Dissipation	T_A=25°C	2.1	W
		T_A=70°C	1.3	
I_{AS}②	Avalanche Current, Single pulse	L=0.1mH	12	A
		L=0.5mH	7	
E_{AS}②	Avalanche Energy, Single pulse	L=0.1mH	7	mJ
		L=0.5mH	12	

Thermal Characteristics

Symbol	Parameter		Rating	Unit
$R_{\theta JC}$	Thermal Resistance-Junction to Case	Steady State	3.4	°C/W
$R_{\theta JA}$③	Thermal Resistance-Junction to Ambient	Steady State	60	°C/W

Note ①：Max. current is limited by junction temperature

Note ②：UIS tested and pulse width are limited by maximum junction temperature 150°C

Note ③：Surface Mounted on 1in² FR-4 board with 1oz

N-Channel Electrical Characteristics (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Electrical Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_{DS}=250uA	100	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=80V, V_{GS}=0V	-	-	1	uA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_{DS}=250uA	1	1.8	3	V
I_{GSS}	Gate Leakage Current	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
$R_{DS(ON)}$④	Drain-Source On-state Resistance	V_{GS}=10V, I_{DS}=10A	-	82	100	mΩ
		V_{GS}=4.5V, I_{DS}=5A	-	87	113	
gfs	Forward Transconductance	V_{DS}=5V, I_{DS}=5A	-	10.5	-	S
Dynamic Characteristics ⑤						
R_G	Gate Resistance	V_{GS}=0V,V_{DS}=0V, Freq.=1MHz	-	6	-	Ω
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=40V, Freq.=1MHz	-	665	-	pF
C_{oss}	Output Capacitance		-	34	-	
C_{rss}	Reverse Transfer Capacitance		-	15	-	
$td_{(ON)}$	Turn-on Delay Time	V_{GS}=10V,V_{DS}=50V, I_D=1A,R_{GEN}=6Ω	-	3.3	-	nS
t_r	Turn-on Rise Time		-	20.3	-	
$t_{d(OFF)}$	Turn-off Delay Time		-	31.4	-	
t_f	Turn-off Fall Time		-	19.8	-	
Q_g	Total Gate Charge	V_{GS}=4.5V,V_{DS}=50V I_D=10A	-	7.25	-	nC
Q_g	Total Gate Charge	V_{GS}=10V,V_{DS}=50V, I_D=10A	-	15.3	-	
Q_{gs}	Gate-Source Charge		-	1.9	-	
Q_{gd}	Gate-Drain Charge		-	2.9	-	
Source-Drain Characteristics						
V_{SD}④	Diode Forward Voltage	I_{SD}=1A, V_{GS}=0V	-	0.7	1.1	V
t_{rr}	Reverse Recovery Time	I_F=1A, V_R=50V dI$_F$/dt=100A/μs	-	17.6	-	nS
Q_{rr}	Reverse Recovery Charge		-	12.6	-	nC

Note ④：Pulse test (pulse width≤300us, duty cycle≤2%).
Note ⑤：Guaranteed by design, not subject to production testing.

N-Channel Typical Characteristics

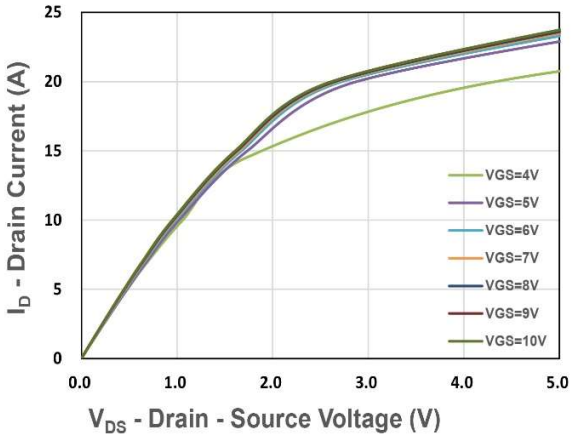


Figure 1. Output Characteristics

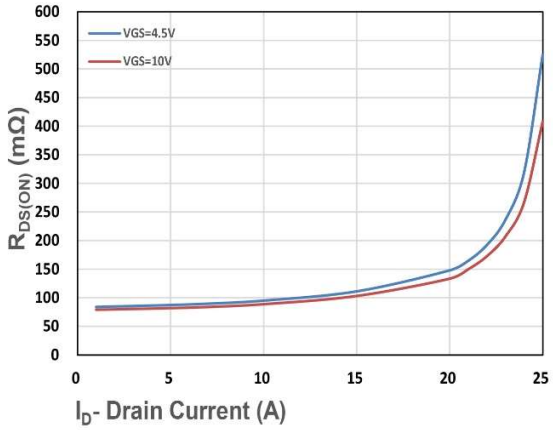


Figure 2. On-Resistance vs. ID

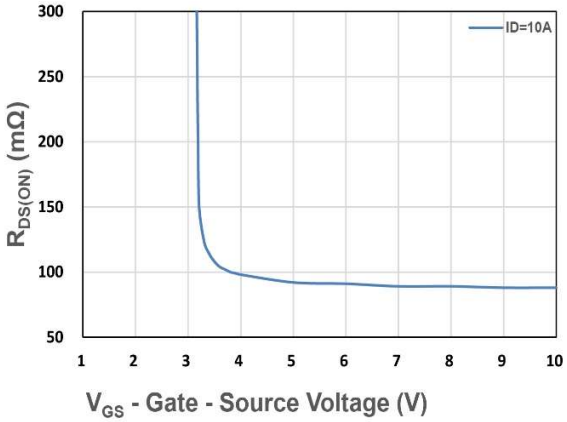


Figure 3. On-Resistance vs. VGS

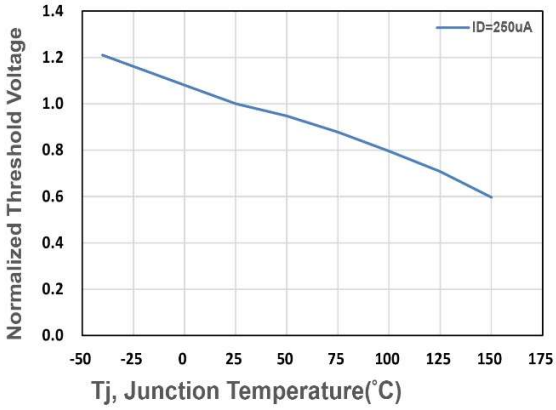


Figure 4. Gate Threshold Voltage

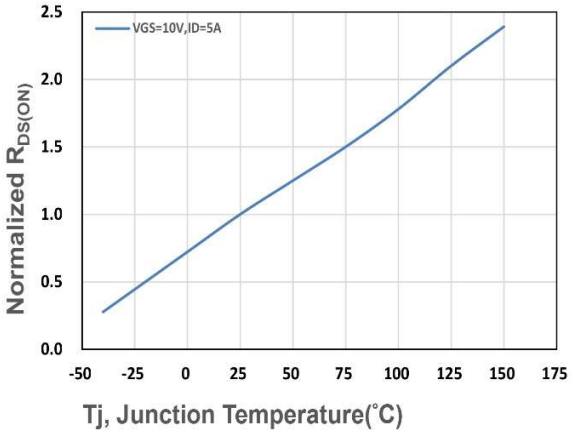


Figure 5. Drain-Source On Resistance

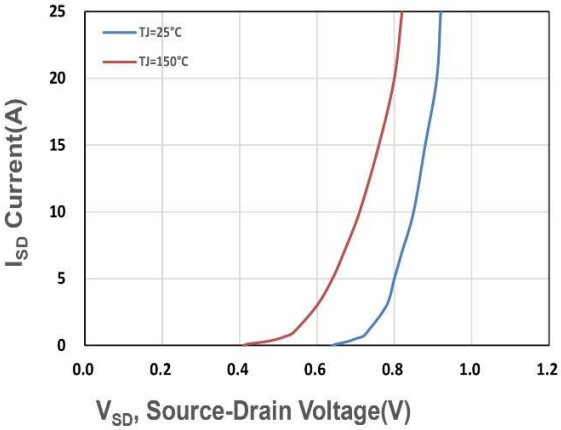


Figure 6. Source-Drain Diode Forward

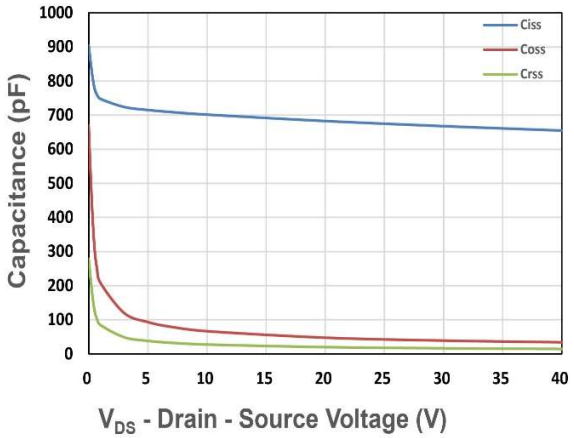


Figure 7. Capacitance

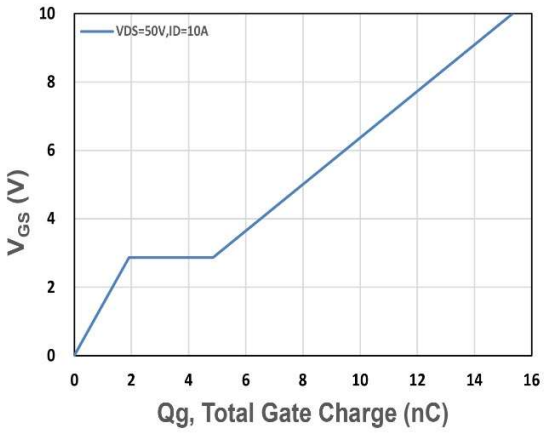


Figure 8. Gate Charge Characteristics

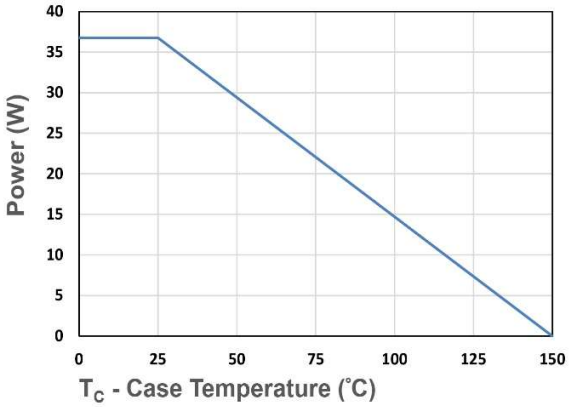


Figure 9. Power Dissipation

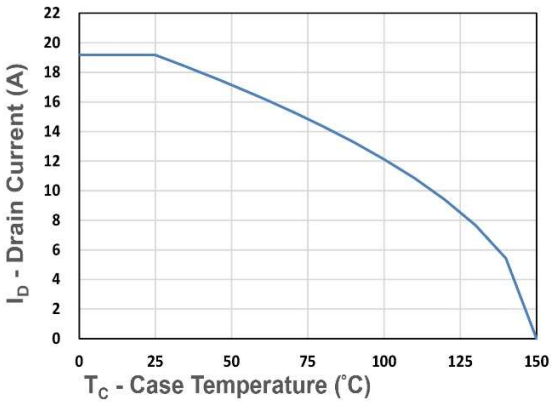


Figure 10. Drain Current

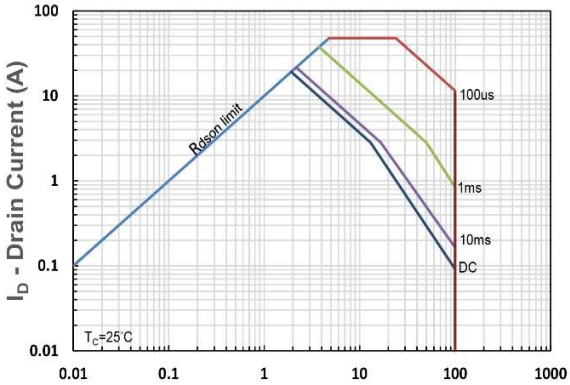


Figure 11. Safe Operating Area

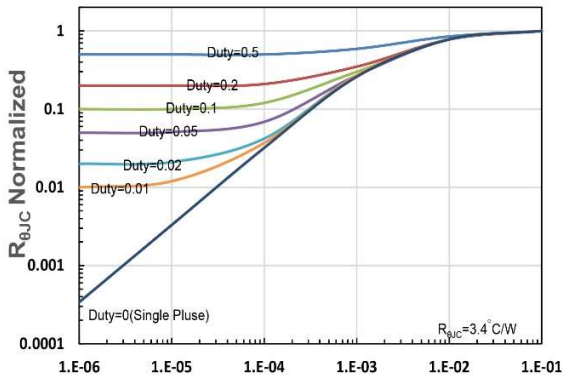


Figure 12. RθJC Transient Thermal Impedance