



Power MOSFETS

DATASHEET

LM1CD40NAI3A

N-Channel
Enhancement Mode MOSFET

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Quality Management Systems

ISO 9001:2015 Certificate

LM1CD40NAI3A



N-Channel Enhancement Mode MOSFET

Pin Description

SOT-23	Symbol	Symbol	N-Channel	Unit
		V_{DS}	120	V
		$R_{DS(ON)-Max}$	440	mΩ
		I_D	1.6	A

Feature

- Fast switching speed
- Reliable and Rugged
- ROHS Compliant & Halogen-Free

Applications

- Power Management in DC/DC Converters
- Motor control
- Disconnect switches

Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM1CD40NAI3A	SOT-23	Tape & Reel	3000 / Tape & Reel	18□□□

Note : □□□□□□ = Lot Code

Absolute Maximum Ratings (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter	N-Channel	Unit
V_{DS}	Drain-Source Voltage	120	V
V_{GS}	Gate-Source Voltage	±20	V
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-55 to 150	°C
I_S	Diode Continuous Forward Current	$T_A=25^{\circ}C$ 1	A
$I_{DM}^{①}$	Pulse Drain Current Tested	$T_A=25^{\circ}C$ 4	A
I_D	Continuous Drain Current	$T_A=25^{\circ}C$ 1.6 $T_A=70^{\circ}C$ 1.3	A
P_D	Maximum Power Dissipation	$T_A=25^{\circ}C$ 1.1 $T_A=70^{\circ}C$ 0.7	W
$I_{AS}^{②}$	Avalanche Current, Single pulse	L=0.1mH 2.5 L=0.5mH 2	A
$E_{AS}^{②}$	Avalanche Energy, Single pulse	L=0.1mH 0.3 L=0.5mH 1	mJ

Thermal Characteristics

Symbol	Parameter	Rating	Unit
$R_{\theta JA}^{③}$	Thermal Resistance-Junction to Ambient	Steady State 110	°C/W

Note ① : Max. current is limited by junction temperature

Note ② : UIS tested and pulse width are limited by maximum junction temperature 150°C

Note ③ : Surface Mounted on 1in² FR-4 board with 1oz

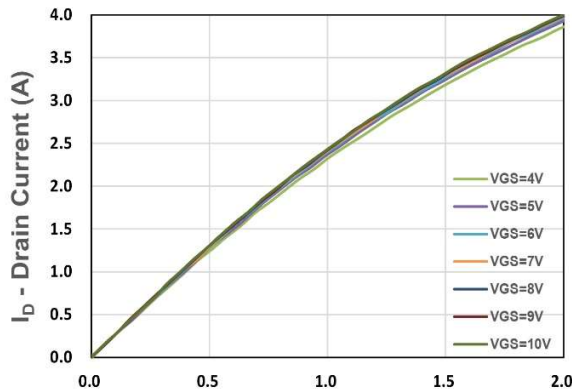
N-Channel Electrical Characteristics (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Electrical Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =250uA	120	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =96V, V _{GS} =0V	-	-	1	uA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =250uA	1	2	3	V
I _{GSS}	Gate Leakage Current	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
R _{DS(ON)} ④	Drain-Source On-state Resistance	V _{GS} =10V, I _{DS} =1A	-	370	440	mΩ
		V _{GS} =4.5V, I _{DS} =0.5A	-	380	495	
gfs	Forward Transconductance	V _{DS} =10V, I _{DS} =0.2A		14	-	S
Dynamic Characteristics ⑤						
R _G	Gate Resistance	V _{GS} =0V, V _{DS} =0V, Freq.=1MHz	-	4.1	-	Ω
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =60V, Freq.=1MHz	-	232	-	pF
C _{oss}	Output Capacitance		-	14	-	
C _{rss}	Reverse Transfer Capacitance		-	9	-	
td(ON)	Turn-on Delay Time	V _{GS} =10V, V _{DS} =25V, Id=1A, RGEN=1Ω	-	4.3	-	nS
tr	Turn-on Rise Time		-	2.6	-	
td(OFF)	Turn-off Delay Time		-	10.9	-	
tf	Turn-off Fall Time		-	11.7	-	
Qg	Total Gate Charge	V _{GS} =4.5V, V _{DS} =60V Id=1A	-	2.5	-	nC
Qg	Total Gate Charge	V _{GS} =10V, V _{DS} =60V, Id=1A	-	5.4	-	
Qgs	Gate-Source Charge		-	1.1	-	
Qgd	Gate-Drain Charge		-	0.7	-	
Source-Drain Characteristics						
VSD④	Diode Forward Voltage	ISD=0.5A, VGS=0V	-	0.75	1.1	V
trr	Reverse Recovery Time	IF=1A, VR=60V	-	20.1	-	nS
Qrr	Reverse Recovery Charge	dIF/dt=100A/μs	-	14.6	-	nC

Note ④ : Pulse test (pulse width≤300us, duty cycle≤2%).

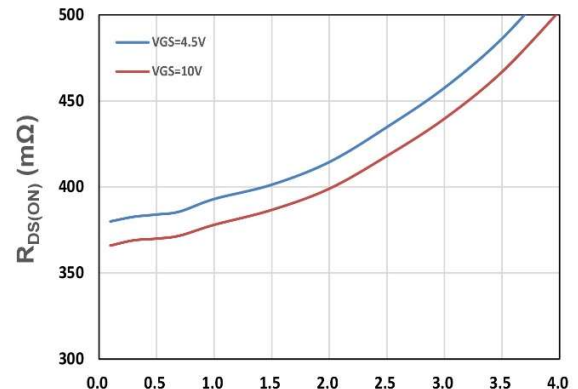
Note ⑤ : Guaranteed by design, not subject to production testing.

N-Channel Typical Characteristics



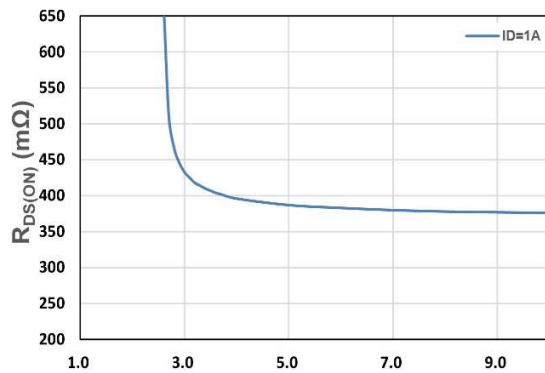
V_{DS} - Drain - Source Voltage (V)

Figure 1. Output Characteristics



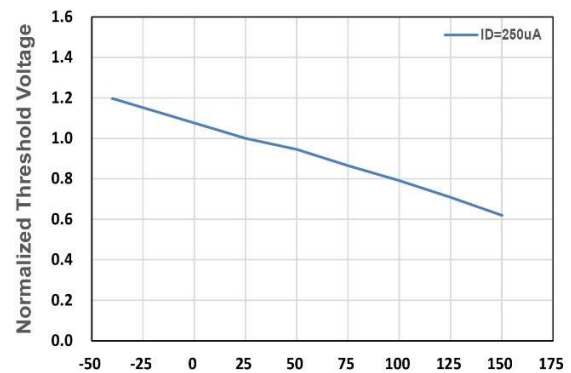
I_D - Drain Current (A)

Figure 2. On-Resistance vs. I_D



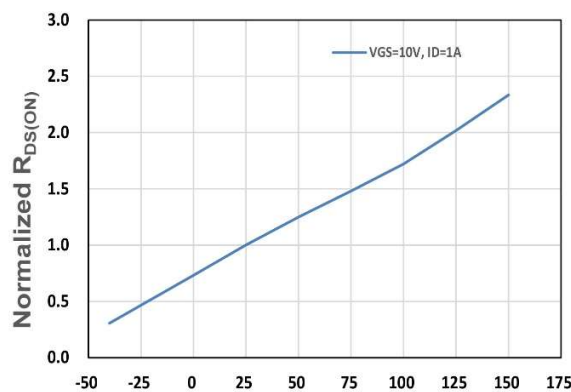
V_{GS} - Gate - Source Voltage (V)

Figure 3. On-Resistance vs. V_{GS}



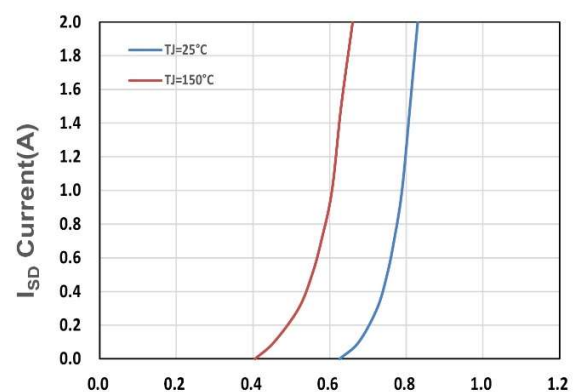
T_j , Junction Temperature(°C)

Figure 4. Gate Threshold Voltage



T_j , Junction Temperature(°C)

Figure 5. Drain-Source On Resistance



V_{SD} , Source-Drain Voltage(V)

Figure 6. Source-Drain Diode Forward

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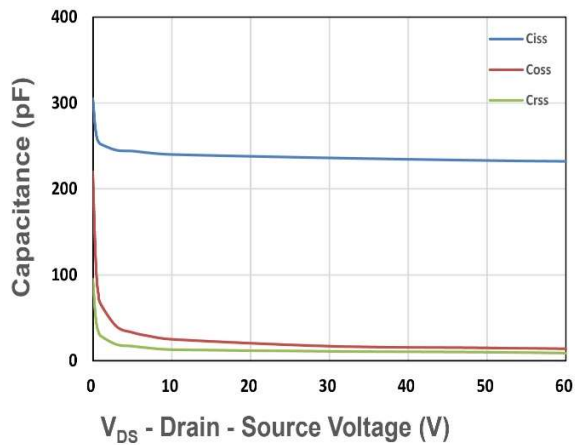


Figure 7. Capacitance

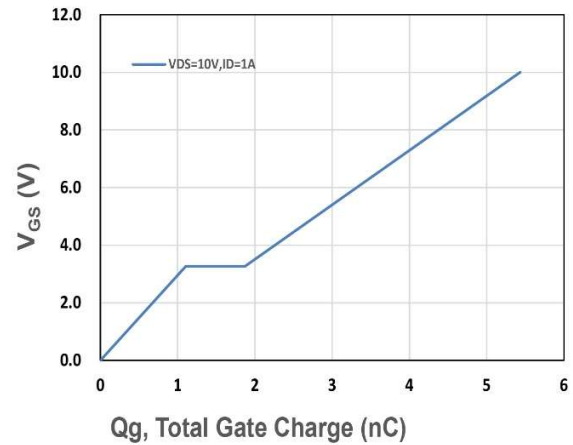


Figure 8. Gate Charge Characteristics

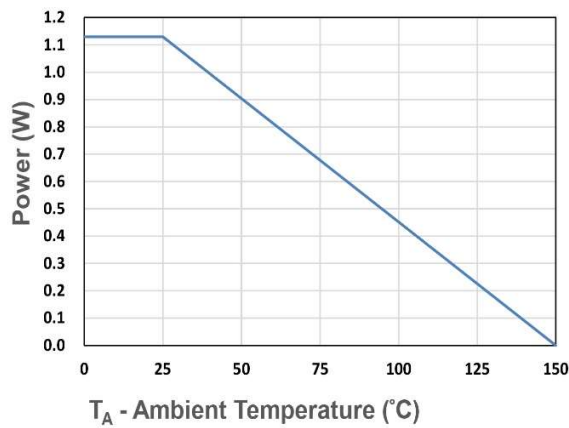


Figure 9. Power Dissipation

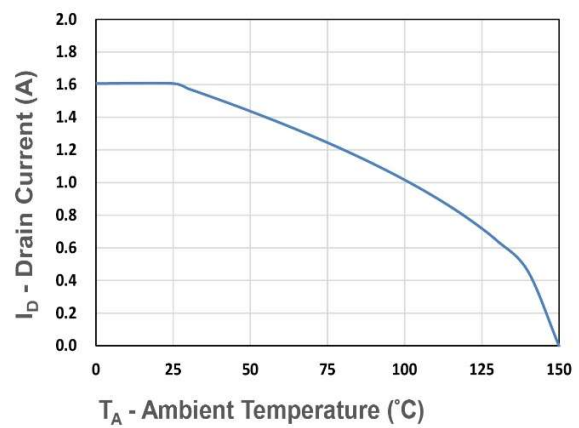


Figure 10. Drain Current

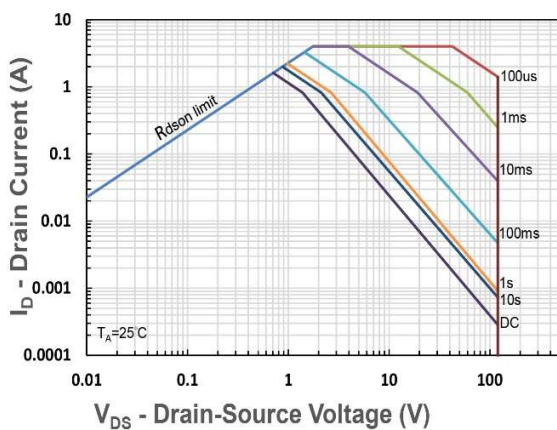


Figure 11. Safe Operating Area

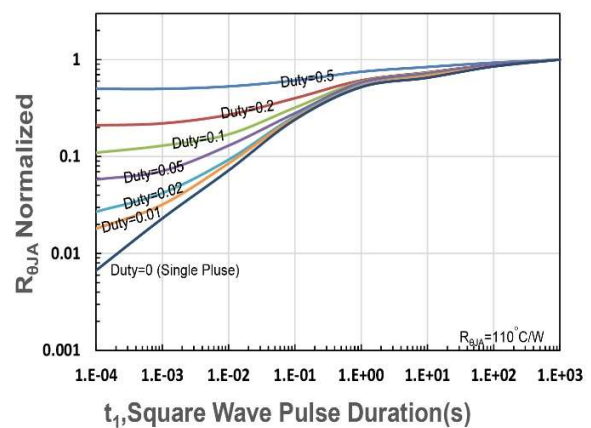


Figure 12. $R_{\theta JA}$ Transient Thermal Impedance