



Power MOSFETS

DATASHEET

LM1F195NHP3A

N-Channel
Enhancement Mode MOSFET

 Leadpower-semiconductor Corp., Ltd

 sales@leadpower-semi.com

 (03) 6577339 FAX : (03) 6577229

 www.leadpower-semi.com

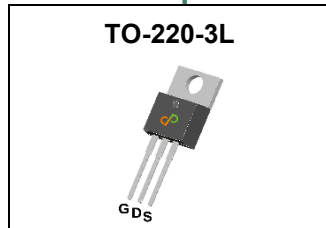


Quality Management Systems

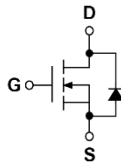
ISO 9001:2015 Certificate

N-Channel Enhancement Mode MOSFET

Pin Description



Symbol



Product Summary

Symbol	N-Channel	Unit
V_{DSS}	150	V
$R_{DS(ON)-Max}$	19.5	mΩ
ID	76	A

Feature

- Fast switching speed
- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- 100% UIS and Rg Tested

Applications

- Synchronous Rectification in SMPS
- Hard Switching and High Speed Circuit
- DC/DC in Telecoms and Industrial

Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM1F195NHP3A	TO-220-3L	Tube	50/ Tube	1F195 □□□□□□

Note : □□□□□□ = Lot Code

Absolute Maximum Ratings ($T_J=25^\circ\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	N-Channel	Unit
V_{DSS}	Drain-Source Voltage	150	V
V_{GSS}	Gate-Source Voltage	± 20	
T_J	Junction Temperature Range	-55 to 150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
I_{SM}	Pulse Drain to Source Diode Forward Current	$T_C=25^\circ\text{C}$	A
I_S	Diode Continuous Forward Current	$T_C=25^\circ\text{C}$	A
$I_{DM}^{(1)}$	Pulse Drain Current Tested	$T_C=25^\circ\text{C}$	A
I_D	Continuous Drain Current	$T_C=25^\circ\text{C}$	A
		$T_C=100^\circ\text{C}$	
P_D	Maximum Power Dissipation	$T_C=25^\circ\text{C}$	W
		$T_C=100^\circ\text{C}$	
I_D	Continuous Drain Current	$T_A=25^\circ\text{C}$	A
		$T_A=70^\circ\text{C}$	
P_D	Maximum Power Dissipation	$T_A=25^\circ\text{C}$	W
		$T_A=70^\circ\text{C}$	
$I_{AS}^{(2)}$	Avalanche Current, Single pulse	L=0.1mH	A
		L=0.5mH	
$E_{AS}^{(2)}$	Avalanche Energy, Single pulse	L=0.1mH	mJ
		L=0.5mH	

Thermal Characteristics

Symbol	Parameter	Rating	Unit
$R_{\theta JC}$	Thermal Resistance-Junction to Case	Steady State	$^\circ\text{C/W}$
$R_{\theta JA}^{(3)}$	Thermal Resistance-Junction to Ambient	Steady State	$^\circ\text{C/W}$

Note ① : Max. current is limited by junction temperature

Note ② : UIS tested and pulse width are limited by maximum junction temperature 150°C

Note ③ : Surface Mounted on 1in² FR-4 board with 1oz

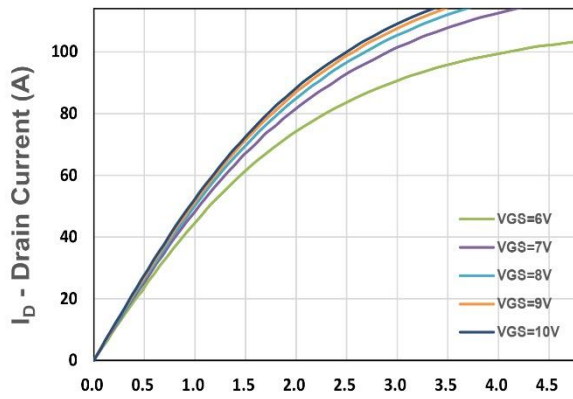
N-Channel Electrical Characteristics ($T_J=25^{\circ}\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Electrical Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =250uA	150	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =120V, V _{GS} =0V	-	-	1	uA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =250uA	2	3	4	V
I _{GSS}	Gate Leakage Current	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
R _{DS(ON)} ④	Drain-Source On-state Resistance	V _{GS} =10V, I _{DS} =20A	-	17.5	19.5	mΩ
gfs	Forward Transconductance	V _{DS} =5V, I _{DS} =10A	-	32.9	-	S
Dynamic Characteristics ⑥						
R _G	Gate Resistance	V _{GS} =0V,V _{DS} =0V, Freq.=1MHz	-	2	-	Ω
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =75V, Freq.=1MHz	-	1892	-	pF
C _{oss}	Output Capacitance		-	141	-	
C _{rss}	Reverse Transfer Capacitance		-	34	-	
td(ON)	Turn-on Delay Time	V _{GS} =10V,V _{DS} =25V, Id=1A,RGEN=1Ω	-	10	-	nS
tr	Turn-on Rise Time		-	3.2	-	
td(OFF)	Turn-off Delay Time		-	21.5	-	
tf	Turn-off Fall Time		-	66.6	-	
Qg	Total Gate Charge	V _{GS} =6V,V _{DS} =75V Id=50A	-	15.2	-	nC
Qg	Total Gate Charge	V _{GS} =10V,V _{DS} =75V, Id=50A	-	24.8	-	
Qgs	Gate-Source Charge		-	11.1	-	
Qgd	Gate-Drain Charge		-	2.87	-	
Source-Drain Characteristics						
VSD④	Diode Forward Voltage	ISD=10A, VGS=0V	-	0.75	1.1	V
trr	Reverse Recovery Time	IF=25A, VR=75V	-	65.9	-	nS
Qrr	Reverse Recovery Charge	dIF/dt=100A/μs	-	130.1	-	nC

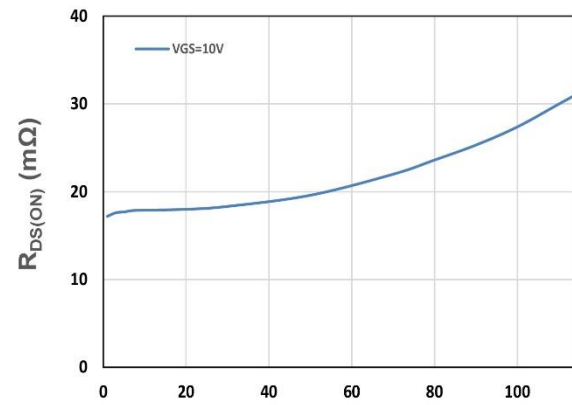
Note ④ : Pulse test (pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$).

Note ⑤ : Guaranteed by design, not subject to production testing.

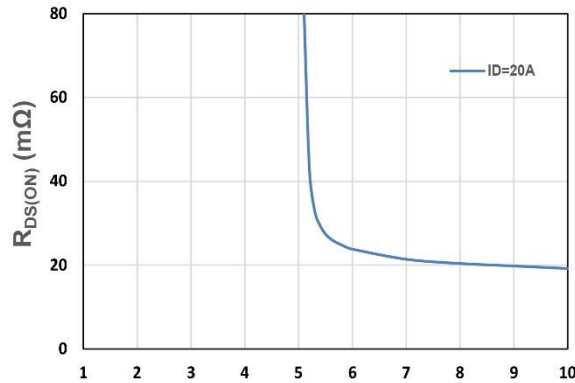
N-Channel Typical Characteristics



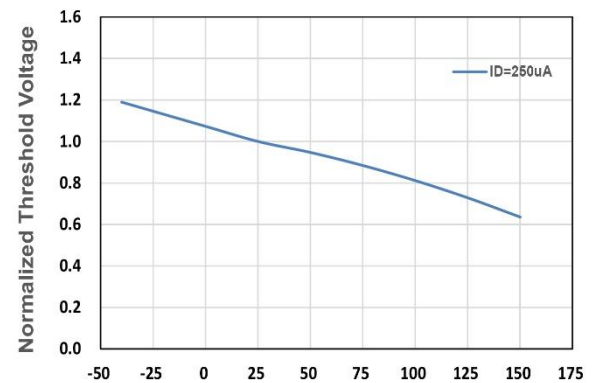
V_{DS} - Drain - Source Voltage (V)
Figure 1. Output Characteristics



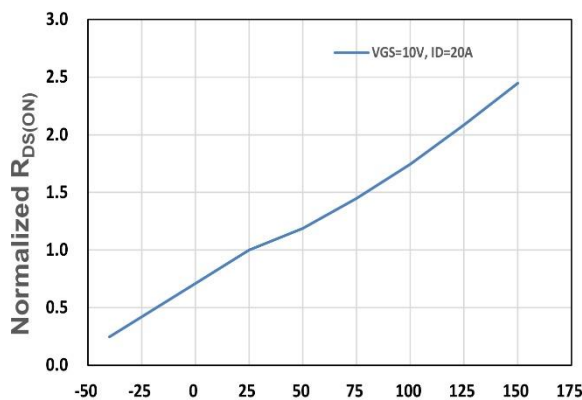
I_D - Drain Current (A)
Figure 2. On-Resistance vs. ID



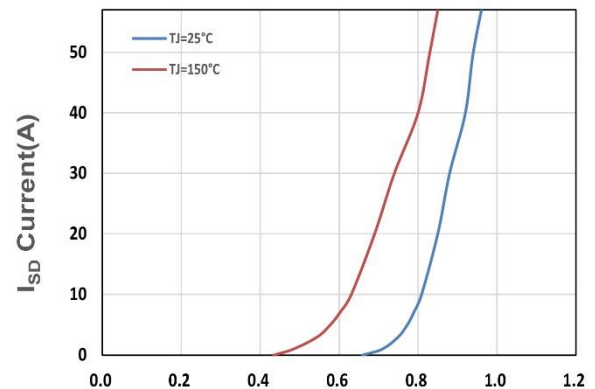
V_{GS} - Gate - Source Voltage (V)
Figure 3. On-Resistance vs. VGS



T_J , Junction Temperature(°C)
Figure 4. Gate Threshold Voltage



T_J , Junction Temperature(°C)
Figure 5. Drain-Source On Resistance



V_{SD} , Source-Drain Voltage(V)
Figure 6. Source-Drain Diode Forward

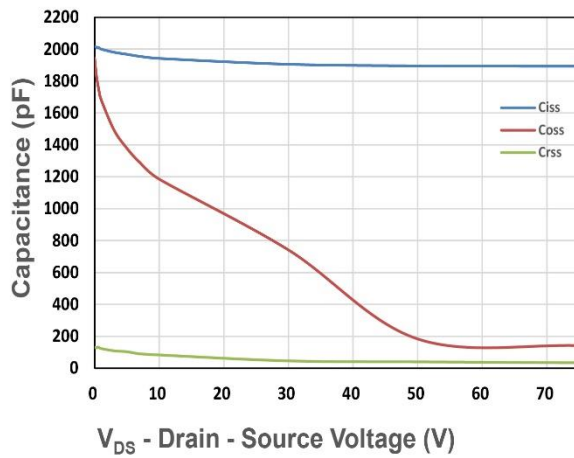


Figure 7. Capacitance

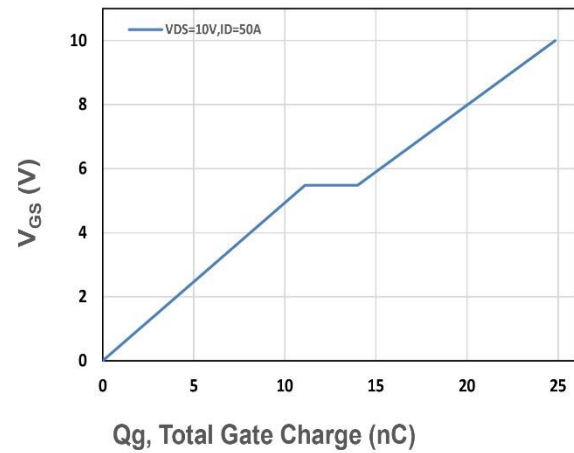


Figure 8. Gate Charge Characteristics

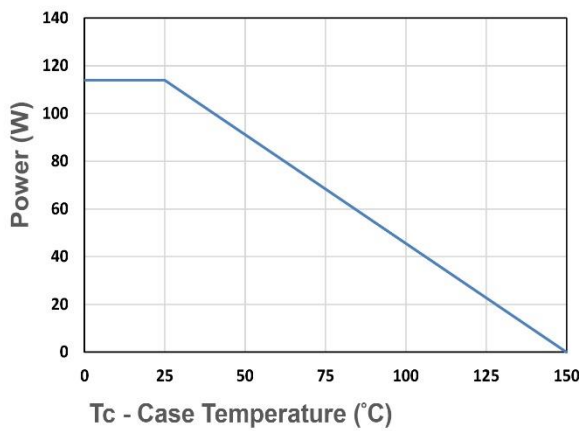


Figure 9. Power Dissipation

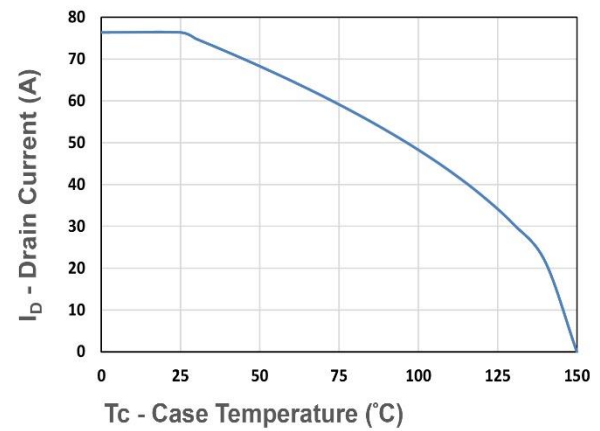


Figure 10. Drain Current

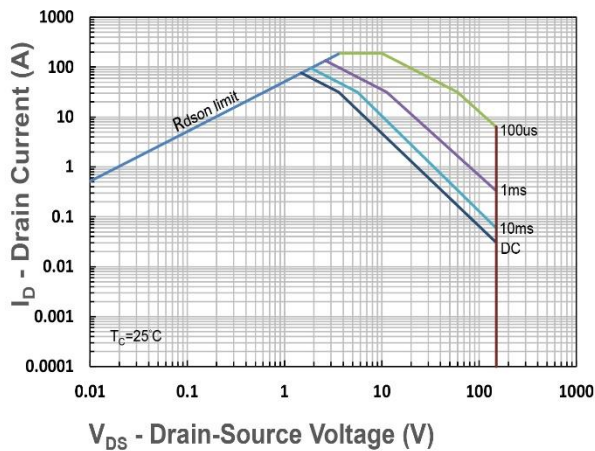


Figure 11. Safe Operating Area

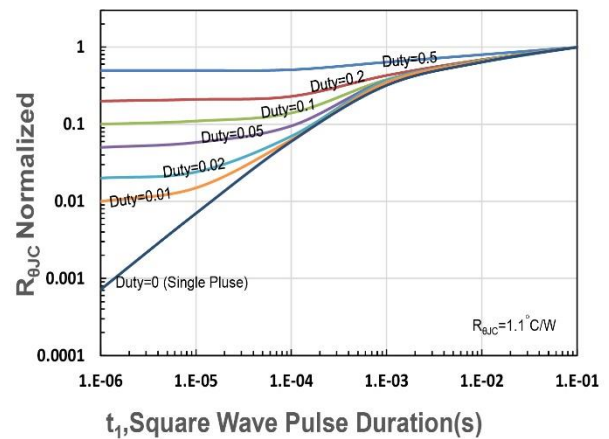


Figure 12. $R_{\theta JC}$ Transient Thermal Impedance