



Power MOSFETS

DATASHEET

LM1F650NAK8A

N-Channel
Enhancement Mode MOSFET

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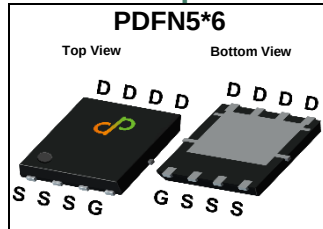


Quality Management Systems

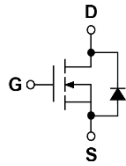
ISO 9001:2015 Certificate

N-Channel Enhancement Mode MOSFET

Pin Description



Symbol



Product Summary

Symbol	N-Channel	Unit
V_{DS}	150	V
$R_{DS(ON)-Max}$	65	m Ω
ID	16	A

Feature

- High Speed Power Switching
- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- 100% UIS Tested

Applications

- Synchronous Rectification in SMPS
- Hard Switching
- Telecoms and Industrial

Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM1F650NAK8A	PDFN5*6	Tape & Reel	5000 / Tape & Reel	1F650 □□□□□□

Note : □□□□□□ = Lot Code

Absolute Maximum Ratings ($T_J=25^\circ\text{C}$ Unless Otherwise Noted)

Symbol	Parameter		N-Channel	Unit
V _{DSS}	Drain-Source Voltage		150	V
V _{GSS}	Gate-Source Voltage		±20	
T _J	Maximum Junction Temperature		150	°C
T _{STG}	Storage Temperature Range		-55 to 150	°C
I _{DM} ^①	Pulse Drain Current Tested	T _c =25°C	38	A
I _D	Continuous Drain Current	T _c =25°C	16	A
		T _c =100°C	10	
P _D	Maximum Power Dissipation	T _c =25°C	36.7	W
		T _c =100°C	14.7	
I _{AS} ^②	Avalanche Current, Single pulse	L=0.1mH	6	A
E _{AS} ^②	Avalanche Energy, Single pulse	L=0.1mH	1.8	mJ

Thermal Characteristics

Symbol	Parameter		Rating	Unit
R _{θJC}	Thermal Resistance-Junction to Case	Steady State	3.4	°C/W
R _{θJA} ^③	Thermal Resistance-Junction to Ambient	Steady State	60	°C/W

Note ① : Max. current is limited by junction temperature

Note ② : UIS tested and pulse width are limited by maximum junction temperature 150°C

Note ③ : Surface Mounted on 1in^2 FR-4 board with 1oz.

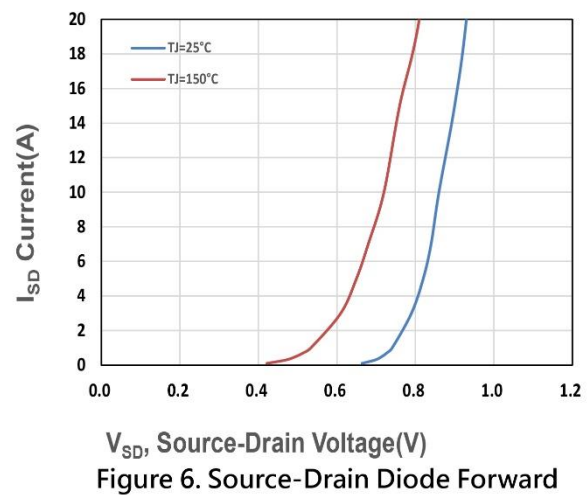
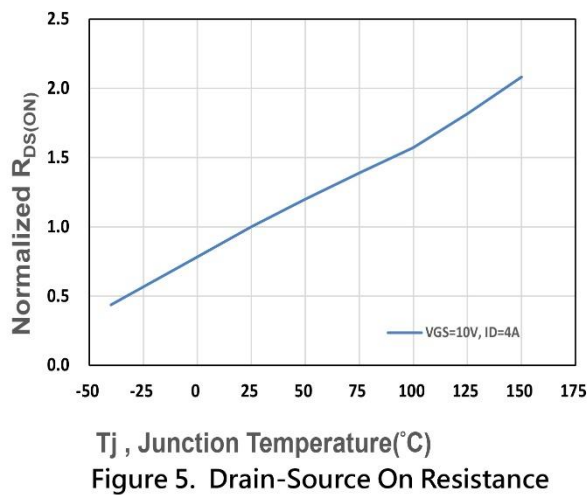
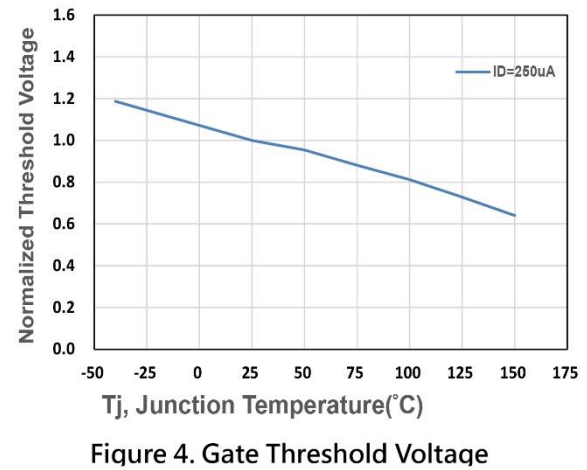
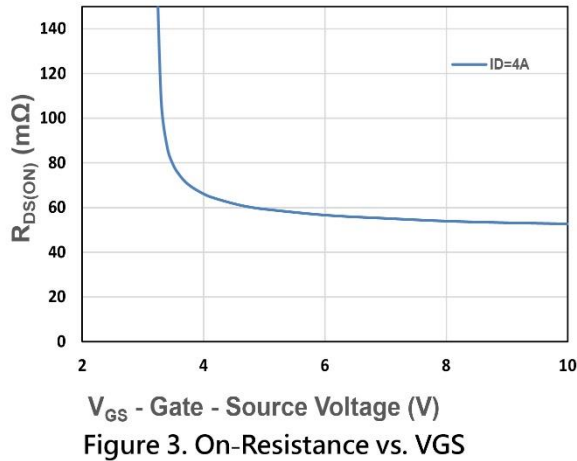
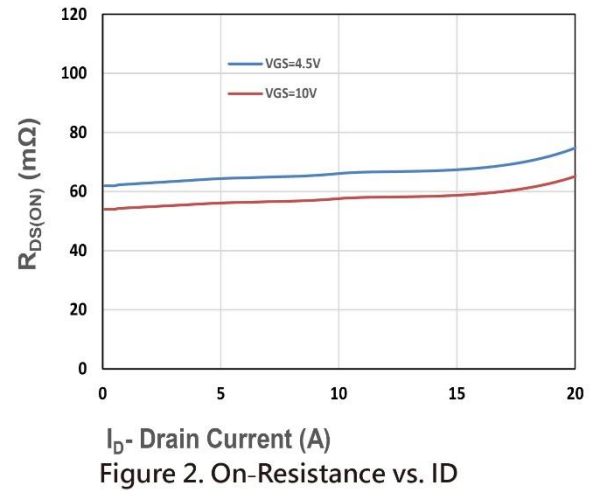
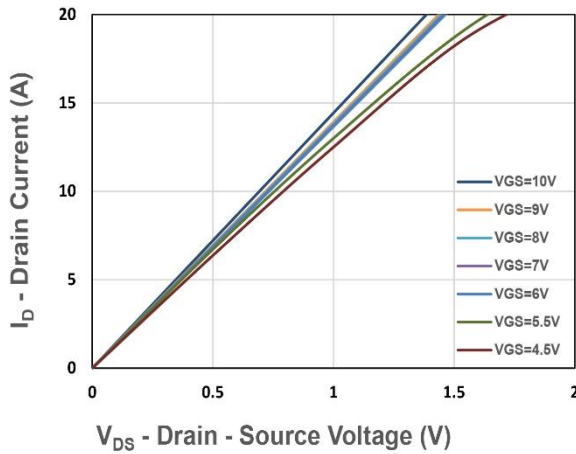
N-Channel Electrical Characteristics ($T_J=25^{\circ}\text{C}$ Unless Otherwise Noted)

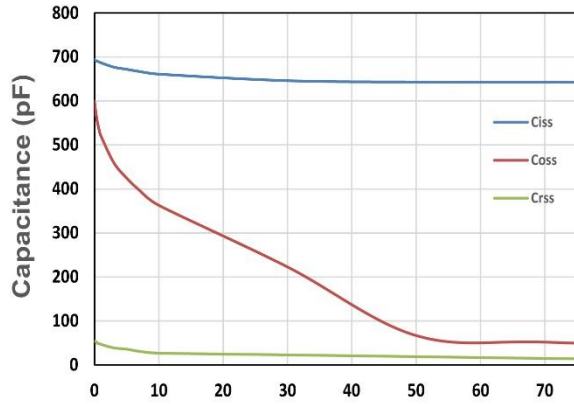
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Electrical Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =250uA	150	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =80V, V _{GS} =0V	-	-	1	uA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =250uA	1	2	3	V
I _{GSS}	Gate Leakage Current	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
R _{DS(ON)} ④	Drain-Source On-state Resistance	V _{GS} =10V, I _{DS} =4A	-	54	65	mΩ
		V _{GS} =4.5V, I _{DS} =3A	-	62	82	
gfs	Forward Transconductance	V _{DS} =5V, I _{DS} =2A	-	5.8	-	S
Dynamic Characteristics ⑥						
R _G	Gate Resistance	V _{GS} =0V, V _{DS} =0V, Freq.=1MHz	-	2	-	Ω
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =75V, Freq.=1MHz	-	642	-	pF
C _{oss}	Output Capacitance		-	50	-	
C _{rss}	Reverse Transfer Capacitance		-	14	-	
td(ON)	Turn-on Delay Time	V _{GS} =10V, V _{DS} =75V, Id=1A, RGEN=1Ω	-	6.3	-	nS
tr	Turn-on Rise Time		-	2.3	-	
td(OFF)	Turn-off Delay Time		-	13.2	-	
tf	Turn-off Fall Time		-	30.3	-	
Qg	Total Gate Charge	V _{GS} =4.5V, V _{DS} =75V Id=4A	-	5.3	-	nC
Qg	Total Gate Charge	V _{GS} =10V, V _{DS} =75V, Id=4A	-	9.9	-	
Qgs	Gate-Source Charge		-	2.8	-	
Qgd	Gate-Drain Charge		-	1	-	
Source-Drain Characteristics						
VSD④	Diode Forward Voltage	ISD=2A, VGS=0V	-	0.75	1.1	V
trr	Reverse Recovery Time	IF=2A, VR=75V	-	42.6	-	nS
Qrr	Reverse Recovery Charge	dIF/dt=100A/μs	-	49.3	-	nC

Note ④ : Pulse test (pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$).

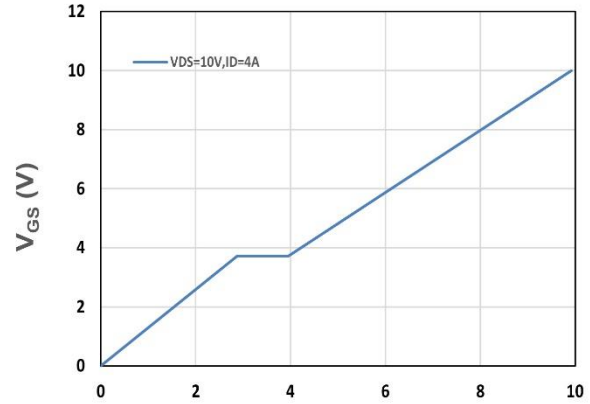
Note ⑤ : Guaranteed by design, not subject to production testing.

N-Channel Typical Characteristics

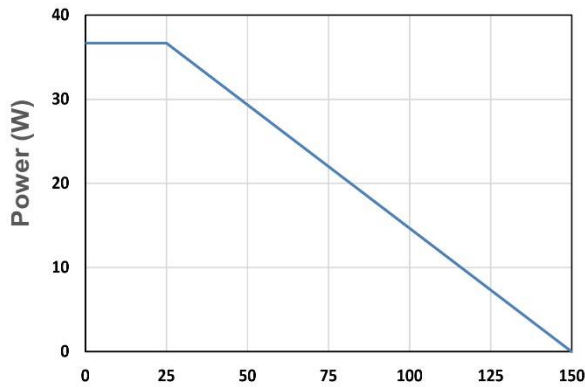




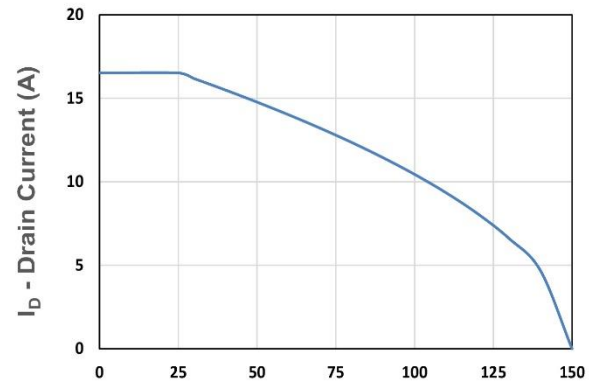
V_{DS} - Drain - Source Voltage (V)
Figure 7. Capacitance



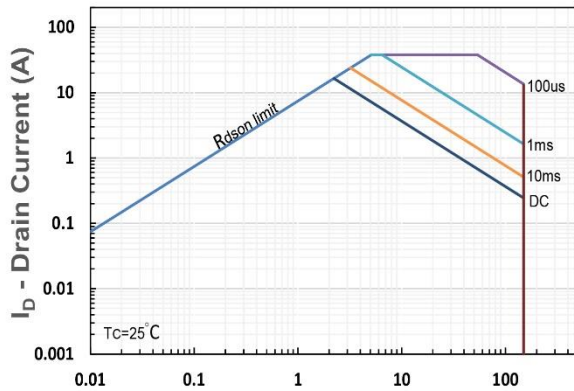
Q_g , Total Gate Charge (nC)
Figure 8. Gate Charge Characteristics



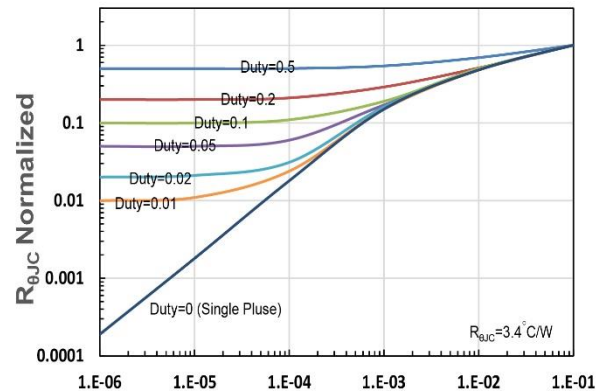
T_c - Case Temperature (°C)
Figure 9. Power Dissipation



T_c - Case Temperature (°C)
Figure 10. Drain Current



V_{DS} - Drain-Source Voltage (V)
Figure 11. Safe Operating Area



t_1 , Square Wave Pulse Duration(s)
Figure 12. $R_{\theta JC}$ Transient Thermal Impedance