



Power MOSFETS

DATASHEET

LM1F650NAQ8A

N-Channel
Enhancement Mode MOSFET

 Leadpower-semiconductor Corp., Ltd

 sales@leadpower-semi.com

 (03) 6577339 FAX : (03) 6577229

 www.leadpower-semi.com

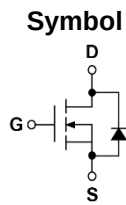


Quality Management Systems

ISO 9001:2015 Certificate

N-Channel Enhancement Mode MOSFET

Pin Description



Product Summary

Symbol	N-Channel	Unit
V_{DS}	150	V
$R_{DS(ON)-Max}$	65	m Ω
ID	3.3	A

Feature

- High Speed Power Switching
- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- 100% UIS Tested

Applications

- Synchronous Rectification in SMPS
- Hard Switching
- Telecoms and Industrial

Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM1F650NAQ8A	SOP-8L	Tape & Reel	3000 / Tape & Reel	1F650 □□□□□□

Note : □□□□□□ = Lot Code

Absolute Maximum Ratings (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter		N-Channel	Unit
V _{DSS}	Drain-Source Voltage		150	V
V _{GSS}	Gate-Source Voltage		±20	
T _J	Maximum Junction Temperature		150	°C
T _{STG}	Storage Temperature Range		-55 to 150	°C
I _{DM} ^①	Pulse Drain Current Tested	T _A =25°C	8.3	A
I _D	Continuous Drain Current	T _A =25°C	3.3	A
		T _A =100°C	2.6	
P _D	Maximum Power Dissipation	T _A =25°C	1.5	W
		T _A =100°C	0.9	
I _{AS} ^②	Avalanche Current, Single pulse	L=0.1mH	6	A
E _{AS} ^②	Avalanche Energy, Single pulse	L=0.1mH	1.8	mJ

Thermal Characteristics

Symbol	Parameter		Rating	Unit
$R_{\theta JA}^{③}$	Thermal Resistance-Junction to Ambient	Steady State	85	°C/W

Note ① : Max. current is limited by junction temperature

Note ② : UIS tested and pulse width are limited by maximum junction temperature 150°C

Note ③ : Surface Mounted on 1in² FR-4 board with 1oz.

N-Channel Electrical Characteristics (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Electrical Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =250uA	150	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =80V, V _{GS} =0V	-	-	1	uA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =250uA	1	2	3	V
I _{GSS}	Gate Leakage Current	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
R _{DS(ON)} ④	Drain-Source On-state Resistance	V _{GS} =10V, I _{DS} =4A	-	54	65	mΩ
		V _{GS} =4.5V, I _{DS} =3A	-	62	82	
gfs	Forward Transconductance	V _{DS} =5V, I _{DS} =2A	-	5.9	-	S
Dynamic Characteristics ⑥						
R _G	Gate Resistance	V _{GS} =0V, V _{DS} =0V, Freq.=1MHz	-	2	-	Ω
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =75V, Freq.=1MHz	-	643	-	pF
C _{oss}	Output Capacitance		-	50	-	
C _{rss}	Reverse Transfer Capacitance		-	15	-	
td(ON)	Turn-on Delay Time	V _{GS} =10V, V _{DS} =75V, I _D =1A, R _{GEN} =1Ω	-	6.2	-	nS
t _r	Turn-on Rise Time		-	2.3	-	
t _{d(OFF)}	Turn-off Delay Time		-	13.3	-	
t _f	Turn-off Fall Time		-	30.3	-	
Q _g	Total Gate Charge	V _{GS} =4.5V, V _{DS} =75V I _D =4A	-	5.3	-	nC
Q _g	Total Gate Charge	V _{GS} =10V, V _{DS} =75V, I _D =4A	-	10	-	
Q _{gs}	Gate-Source Charge		-	2.8	-	
Q _{gd}	Gate-Drain Charge		-	1.05	-	
Source-Drain Characteristics						
V _{SD} ④	Diode Forward Voltage	I _{SD} =2A, V _{GS} =0V	-	0.8	1.1	V
t _{rr}	Reverse Recovery Time	I _F =2A, V _R =75V	-	42.5	-	nS
Q _{rr}	Reverse Recovery Charge	dI _F /dt=100A/μs	-	49.5	-	nC

Note ④ : Pulse test (pulse width≤300us, duty cycle≤2%).

Note ⑤ : Guaranteed by design, not subject to production testing.

N-Channel Typical Characteristics

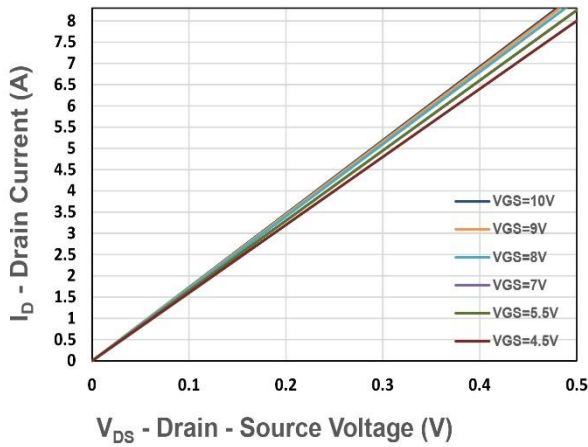


Figure 1. Output Characteristics

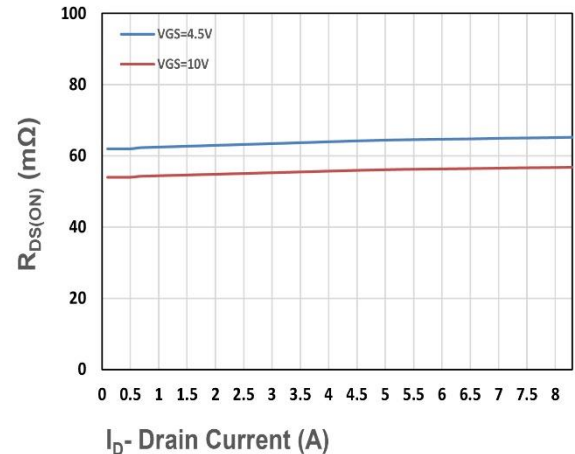


Figure 2. On-Resistance vs. ID

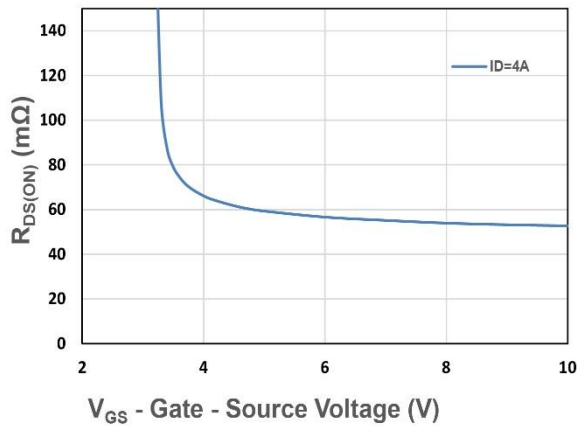


Figure 3. On-Resistance vs. VGS

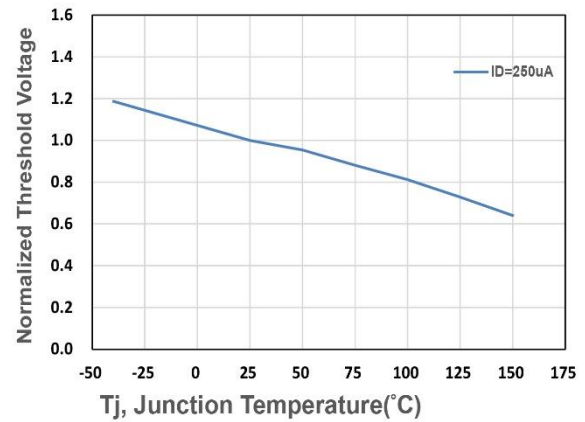


Figure 4. Gate Threshold Voltage

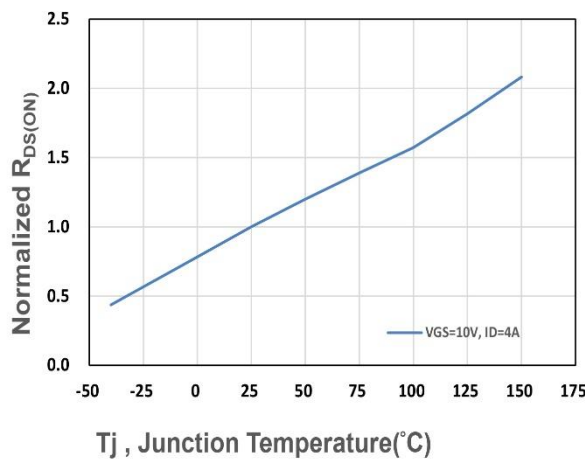


Figure 5. Drain-Source On Resistance

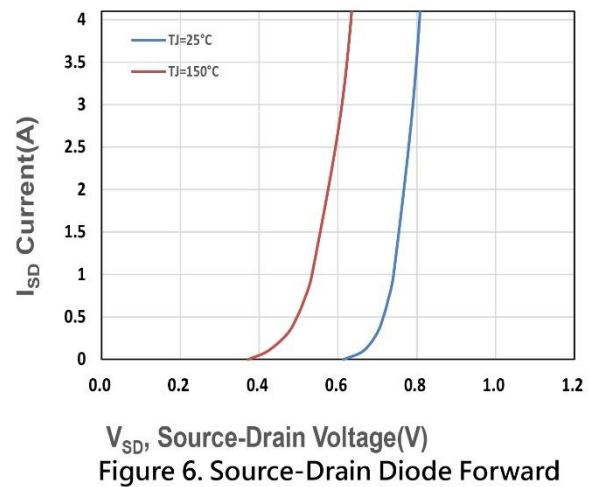
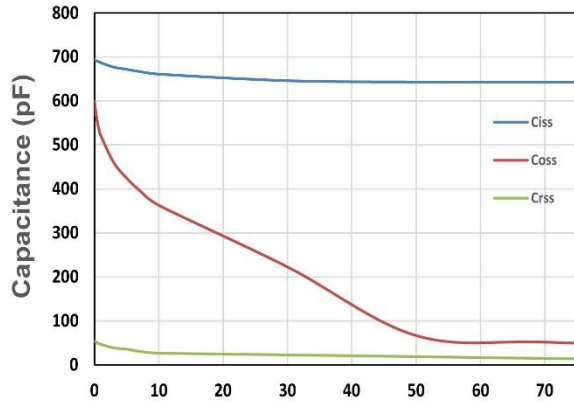
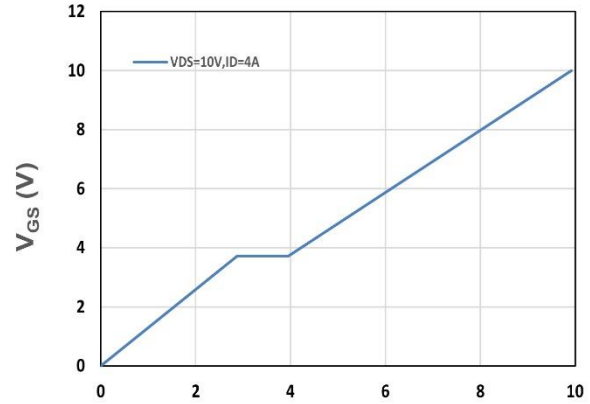


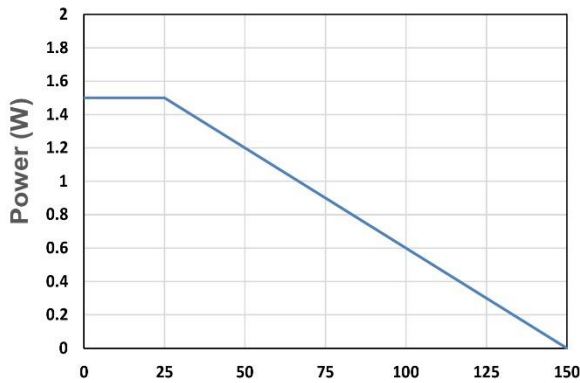
Figure 6. Source-Drain Diode Forward



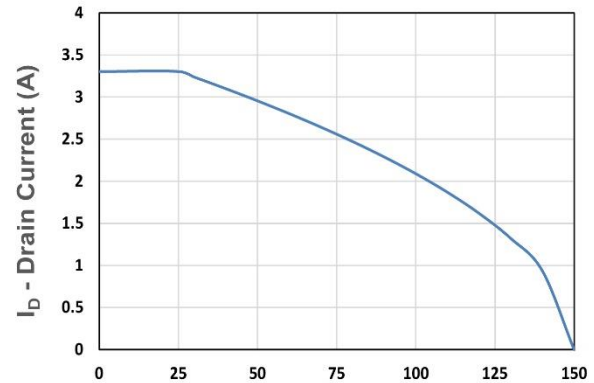
V_{DS} - Drain - Source Voltage (V)
Figure 7. Capacitance



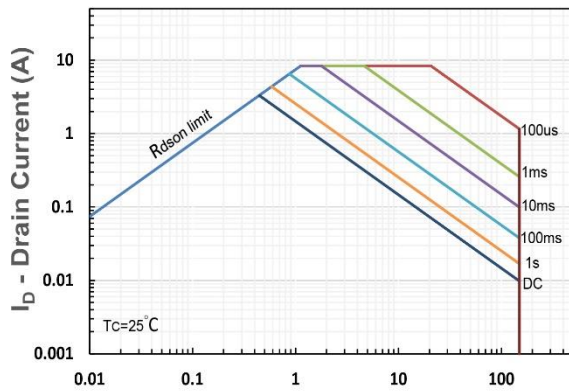
Q_g , Total Gate Charge (nC)
Figure 8. Gate Charge Characteristics



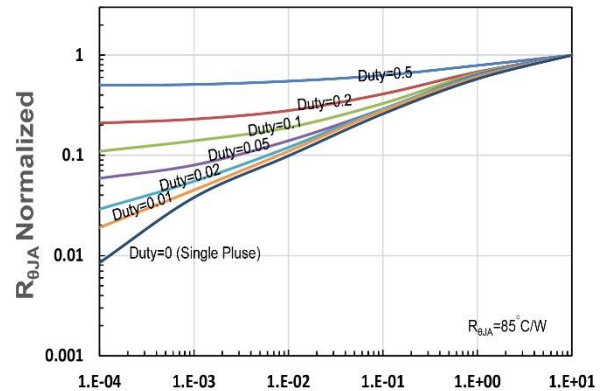
T_A - Ambient Temperature (°C)
Figure 9. Power Dissipation



T_A - Ambient Temperature (°C)
Figure 10. Drain Current



V_{DS} - Drain-Source Voltage (V)
Figure 11. Safe Operating Area



t_1 , Square Wave Pulse Duration(s)
Figure 12. $R_{\theta JA}$ Transient Thermal Impedance