



Power MOSFETS

DATASHEET

LM1FB80NAO2A

N-Channel
Enhancement Mode MOSFET

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Quality Management Systems

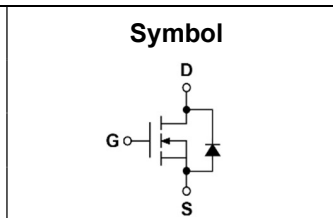
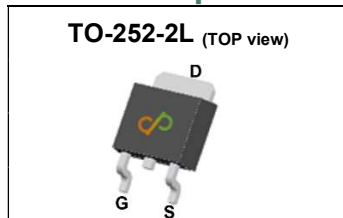
ISO 9001:2015 Certificate

LM1FB80NAO2A



N-Channel Enhancement Mode MOSFET

Pin Description



Ordering Information

Symbol	N-Channel	Unit
V_{DSS}	150	V
$R_{DS(ON)-Max}$	255	mΩ
I_D	7.7	A

Feature

- Fast switching speed
- Reliable and Rugged
- ROHS Compliant & Halogen-Free

Applications

- DC-DC converter switching for Networking
- General purpose switching

Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM1FB80NAO2A	TO-252-2L	Tape & Reel	3000 / Tape & Reel	1FB80 □□□□□□

Note : □□□□□□ = Lot Code

Absolute Maximum Ratings (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter		N-Channel	Unit
V_{DSS}	Drain-Source Voltage		150	V
V_{GSS}	Gate-Source Voltage		±20	
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature Range		-55 to 150	°C
$I_{DM}^{①}$	Pulse Drain Current Tested	$T_c=25^{\circ}C$	19	A
I_D	Continuous Drain Current	$T_c=25^{\circ}C$	7.7	A
		$T_c=100^{\circ}C$	4.9	
P_D	Maximum Power Dissipation	$T_c=25^{\circ}C$	37	W
		$T_c=100^{\circ}C$	15	
$I_{AS}^{②}$	Avalanche Current, Single pulse	$L=0.1mH$	2	A
$E_{AS}^{②}$	Avalanche Energy, Single pulse	$L=0.1mH$	0.2	mJ

Thermal Characteristics

Symbol	Parameter		Rating	Unit
$R_{\theta JC}$	Thermal Resistance-Junction to Case	Steady State	3.4	°C/W
$R_{\theta JA}^{③}$	Thermal Resistance-Junction to Ambient	Steady State	60	°C/W

Note ① : Max. current is limited by junction temperature

Note ② : UIS tested and pulse width are limited by maximum junction temperature 150°C

Note ③ : Surface Mounted on 1in² FR-4 board with 1oz.

N-Channel Electrical Characteristics (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Electrical Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =250uA	150	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =120V, V _{GS} =0V	-	-	1	uA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =250uA	1.2	2	2.5	V
I _{GSS}	Gate Leakage Current	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
R _{DS(ON)} ^④	Drain-Source On-state Resistance	V _{GS} =10V, I _{DS} =1A	-	215	255	mΩ
		V _{GS} =4.5V, I _{DS} =0.5A	-	220	280	
gfs	Forward Transconductance	V _{DS} =5V, I _{DS} =0.5A	-	4.55	-	S
Dynamic Characteristics ^⑤						
R _G	Gate Resistance	V _{GS} =0V, V _{DS} =0V, Freq.=1MHz	-	9	-	Ω
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =75V, Freq.=1MHz	-	712	-	pF
C _{oss}	Output Capacitance		-	19	-	
C _{rss}	Reverse Transfer Capacitance		-	7.8	-	
td(ON)	Turn-on Delay Time	V _{GS} =10V, V _{DS} =75V, I _D =1A, R _{GEN} =6Ω	-	11	-	nS
t _r	Turn-on Rise Time		-	6	-	
t _{d(OFF)}	Turn-off Delay Time		-	24	-	
t _f	Turn-off Fall Time		-	6	-	
Q _g	Total Gate Charge	V _{GS} =4.5V, V _{DS} =75V I _D =1A	-	6.3	-	nC
Q _g	Total Gate Charge	V _{GS} =10V, V _{DS} =75V, I _D =1A	-	13	-	
Q _{gs}	Gate-Source Charge		-	1.86	-	
Q _{gd}	Gate-Drain Charge		-	2.4	-	
Source-Drain Characteristics						
V _{SD} ^④	Diode Forward Voltage	I _{SD} =1A, V _{GS} =0V	-	0.75	1.1	V
t _{rr}	Reverse Recovery Time	I _F =1A, V _R =75V	-	30	-	nS
Q _{rr}	Reverse Recovery Charge	dI _F /dt=100A/μs	-	15	-	nC

Note ④ : Pulse test (pulse width≤300us, duty cycle≤2%).

Note ⑤ : Guaranteed by design, not subject to production testing.

N-Channel Typical Characteristics

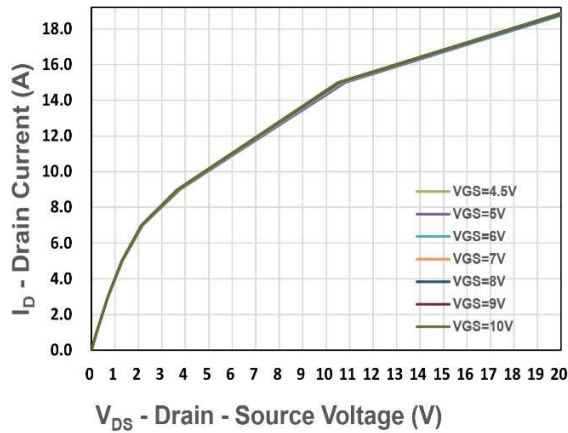


Figure 1. Output Characteristics

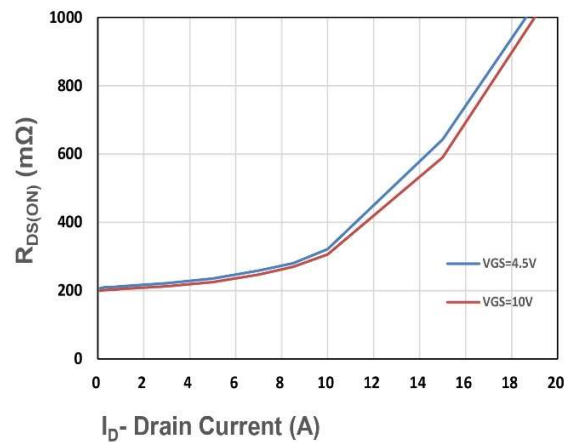


Figure 2. On-Resistance vs. ID

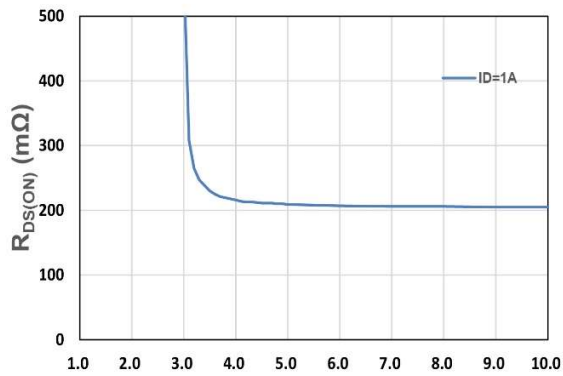


Figure 3. On-Resistance vs. VGS

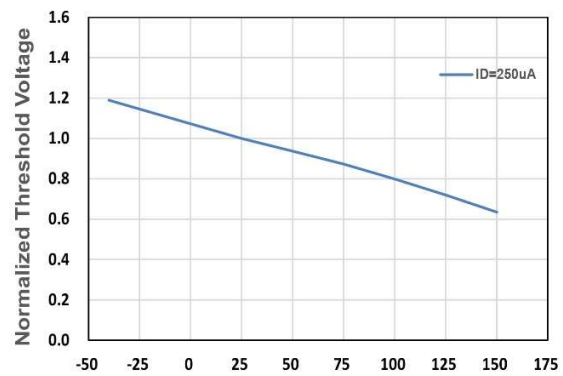


Figure 4. Gate Threshold Voltage

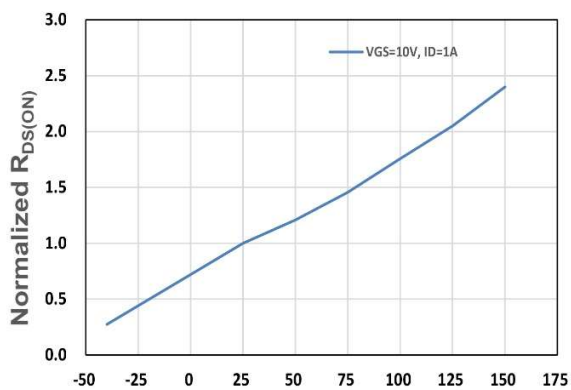


Figure 5. Drain-Source On Resistance

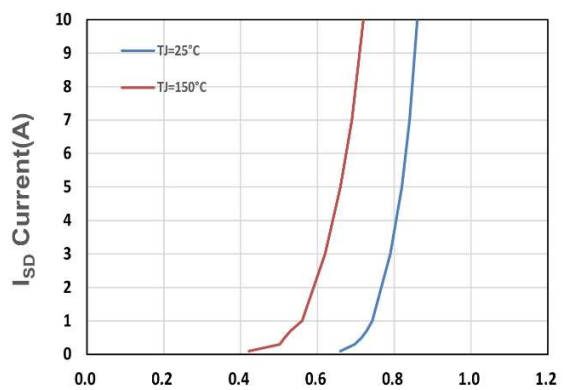
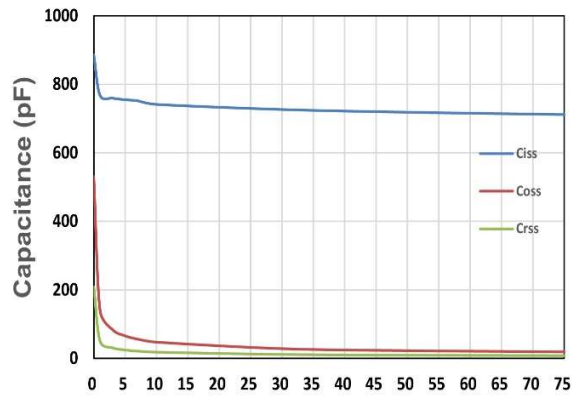
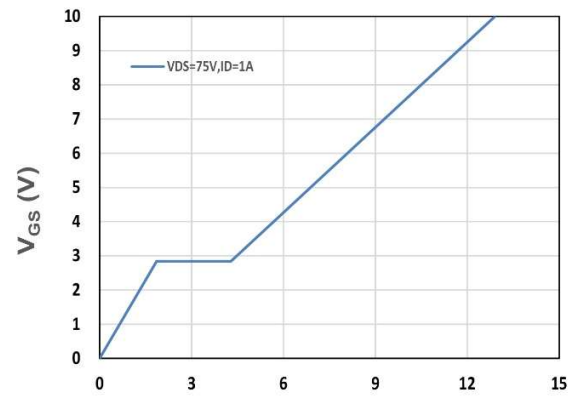


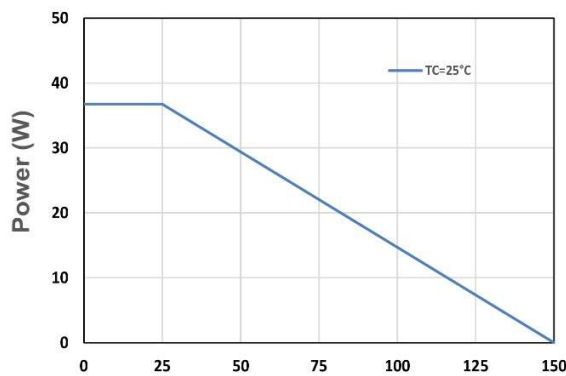
Figure 6. Source-Drain Diode Forward



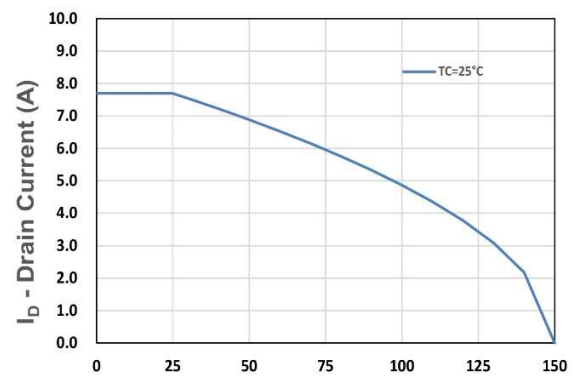
V_{DS} - Drain - Source Voltage (V)
Figure 7. Capacitance



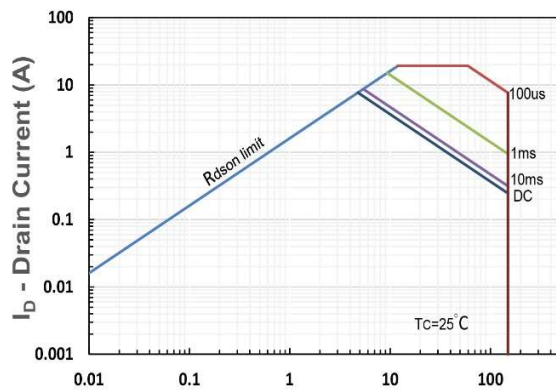
Qg , Total Gate Charge (nC)
Figure 8. Gate Charge Characteristics



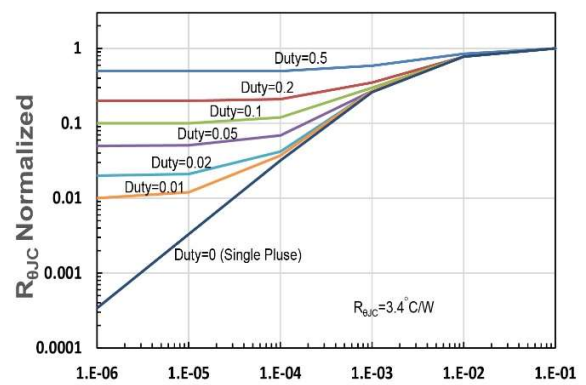
Tj - Junction Temperature (°C)
Figure 9. Power Dissipation



Tj - Junction Temperature (°C)
Figure 10. Drain Current



V_{DS} - Drain-Source Voltage (V)
Figure 11. Safe Operating Area



t_1 , Square Wave Pulse Duration(s)
Figure 12. $R_{\theta JC}$ Transient Thermal Impedance