



Power MOSFETS

DATASHEET

LM20F40PGA3A

N-Channel
Enhancement Mode MOSFET

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Quality Management Systems
ISO 9001:2015 Certificate

P-Channel Enhancement Mode MOSFET

Pin Description

FBP1006 (TOP view)	Symbol	Symbol	P-Channel	Unit
		V_{DSS}	-20	V
		$R_{DS(ON)-Max}$	640	$\text{m}\Omega$
		ID	-0.85	A

Feature

- Surface mount package
- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- ESD Protection

Applications

- Small Signal Switch
- Load Switch

Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM20F40PGA3A	FBP1006	Tape & Reel	10000 / Tape & Reel	<input type="checkbox"/> 4

Absolute Maximum Ratings ($T_J=25^\circ\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	P-Channel	Unit	
V_{DSS}	Drain-Source Voltage	-20	V	
V_{GSS}	Gate-Source Voltage	± 12		
T_J	Maximum Junction Temperature	150	$^\circ\text{C}$	
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$	
$I_{DM}^{\text{(1)}}$	Pulse Drain Current Tested	$T_A=25^\circ\text{C}$	-2.1	A
I_D	Continuous Drain Current	$T_A=25^\circ\text{C}$	-0.85	A
		$T_A=70^\circ\text{C}$	-0.68	
P_D	Maximum Power Dissipation	$T_A=25^\circ\text{C}$	0.69	W
		$T_A=70^\circ\text{C}$	0.44	

Thermal Characteristics

Symbol	Parameter	Rating	Unit	
$R_{\theta JA}^{\text{(2)}}$	Thermal Resistance-Junction to Ambient	Steady State	180	$^\circ\text{C}/\text{W}$

Note ① : Max. current is limited by junction temperature.

Note ② : Surface Mounted on 1in² FR-4 board with 1oz.

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P-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Electrical Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}$, $I_{\text{DS}}=-250\mu\text{A}$	-20	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{\text{DS}}=-16\text{V}$, $V_{\text{GS}}=0\text{V}$	-	-	-1	μA
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}$, $I_{\text{DS}}=-250\mu\text{A}$	-0.5	-0.75	-1	V
I_{GSS}	Gate Leakage Current	$V_{\text{GS}}=\pm 12\text{V}$, $V_{\text{DS}}=0\text{V}$	-	-	± 10	μA
$R_{\text{DS(ON)}}^{\circledast}$	Drain-Source On-state Resistance	$V_{\text{GS}}=-4.5\text{V}$, $I_{\text{DS}}=-550\text{mA}$	-	530	640	$\text{m}\Omega$
		$V_{\text{GS}}=-2.5\text{V}$, $I_{\text{DS}}=-450\text{mA}$	-	730	950	
		$V_{\text{GS}}=-1.8\text{V}$, $I_{\text{DS}}=-350\text{mA}$	-	1300	1950	
g_{fs}	Forward Transconductance	$V_{\text{DS}}=-5\text{V}$, $I_{\text{DS}}=-550\text{mA}$	-	1	-	S
Dynamic Characteristics ^④						
C_{iss}	Input Capacitance	$V_{\text{GS}}=0\text{V}$, $V_{\text{DS}}=-10\text{V}$, Freq.=1MHz	-	58	-	pF
C_{oss}	Output Capacitance		-	5.7	-	
C_{rss}	Reverse Transfer Capacitance		-	4.4	-	
$t_{\text{d(ON)}}$	Turn-on Delay Time	$V_{\text{GS}}=-4.5\text{V}$, $V_{\text{DS}}=-10\text{V}$, $I_{\text{D}}=-1\text{A}$, $R_{\text{GEN}}=6\Omega$	-	0.4	-	uS
t_{r}	Turn-on Rise Time		-	0.06	-	
$t_{\text{d(OFF)}}$	Turn-off Delay Time		-	0.02	-	
t_{f}	Turn-off Fall Time		-	0.8	-	
Q_{g}	Total Gate Charge	$V_{\text{GS}}=-2.5\text{V}$, $V_{\text{DS}}=-10\text{V}$ $I_{\text{D}}=-1\text{A}$	-	0.53	-	nC
Q_{g}	Total Gate Charge	$V_{\text{GS}}=-4.5\text{V}$, $V_{\text{DS}}=-10\text{V}$, $I_{\text{D}}=-1\text{A}$	-	0.8	-	
Q_{gs}	Gate-Source Charge		-	0.2	-	
Q_{gd}	Gate-Drain Charge		-	0.2	-	
Source-Drain Characteristics						
$V_{\text{SD}}^{\circledast}$	Diode Forward Voltage	$I_{\text{SD}}=-1\text{A}$, $V_{\text{GS}}=0\text{V}$	-	-0.75	-1.1	V
t_{rr}	Reverse Recovery Time	$I_{\text{F}}=-1\text{A}$, $V_{\text{R}}=0\text{V}$ $dI_{\text{F}}/dt=100\text{A}/\mu\text{s}$	-	9.2	-	nS
Q_{rr}	Reverse Recovery Charge		-	0.8	-	nC

Note ④ : Pulse test (pulse width $\leq 300\text{us}$, duty cycle $\leq 2\%$).

Note ⑤ : Guaranteed by design, not subject to production testing.

P-Channel Typical Characteristics

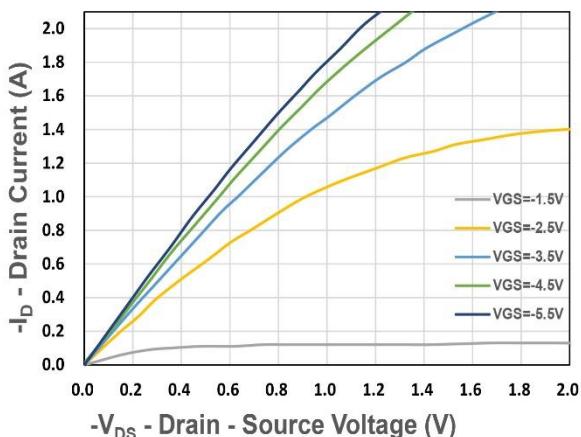


Figure 1. Output Characteristics

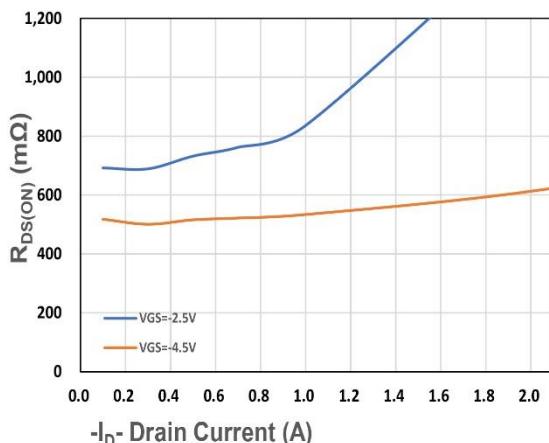


Figure 2. On-Resistance vs. ID

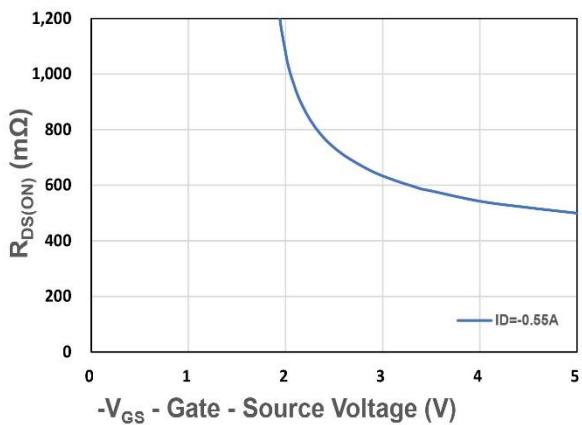


Figure 3. On-Resistance vs. VGS

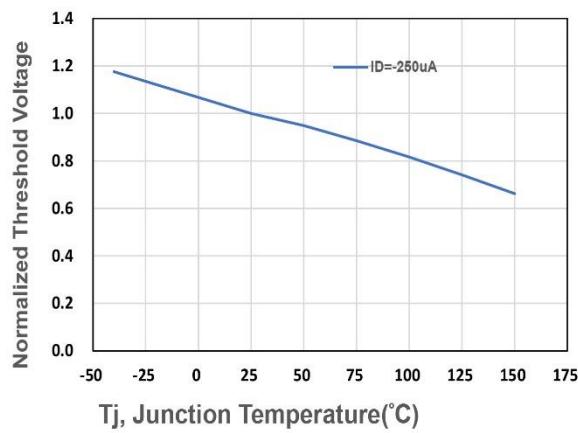


Figure 4. Gate Threshold Voltage

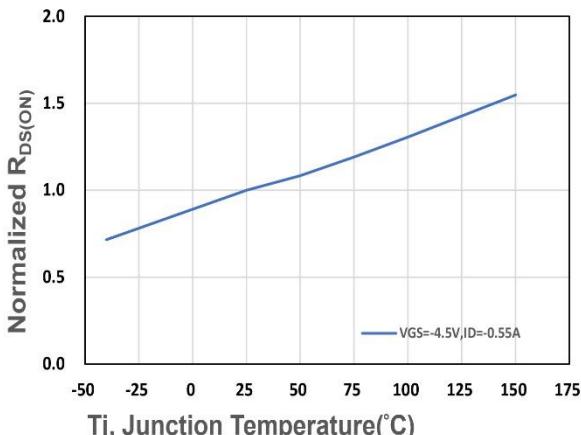


Figure 5. Drain-Source On Resistance

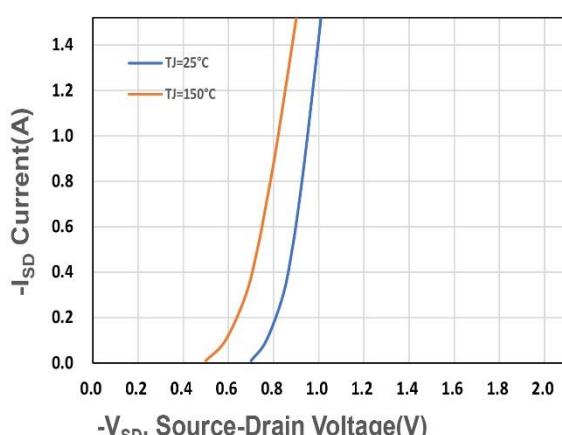


Figure 6. Source-Drain Diode Forward

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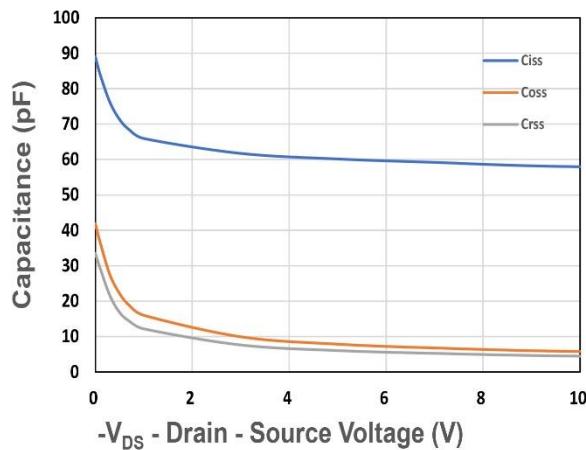


Figure 7. Capacitance

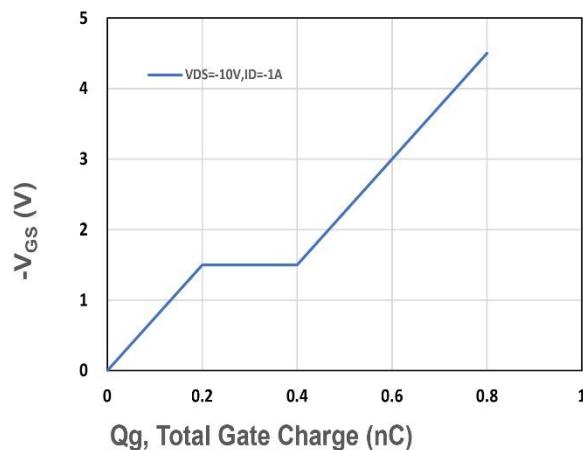


Figure 8. Gate Charge Characteristics

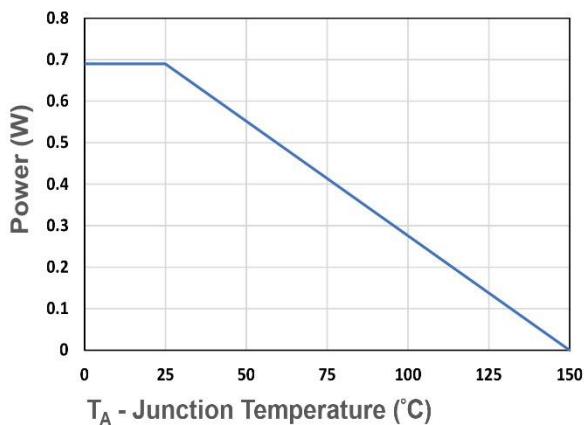


Figure 9. Power Dissipation

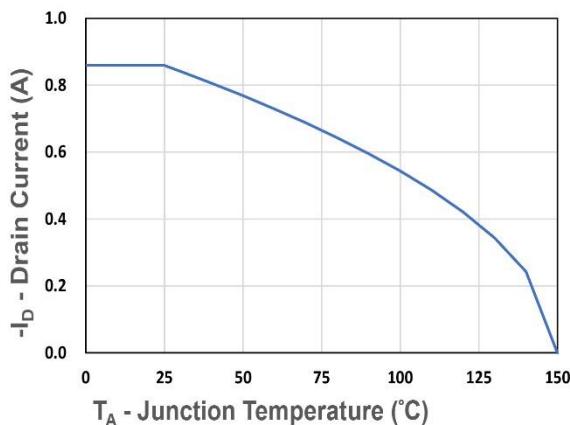


Figure 10. Drain Current

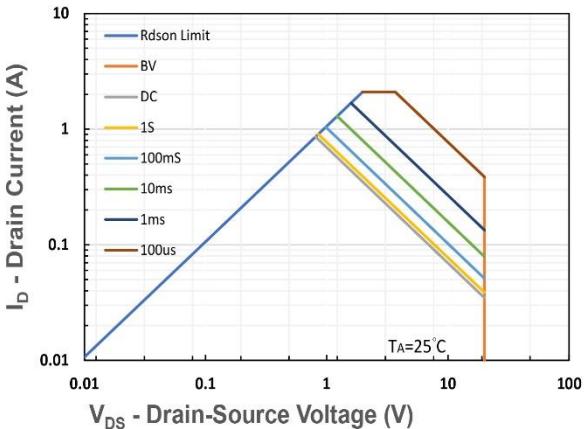


Figure 11. Safe Operating Area

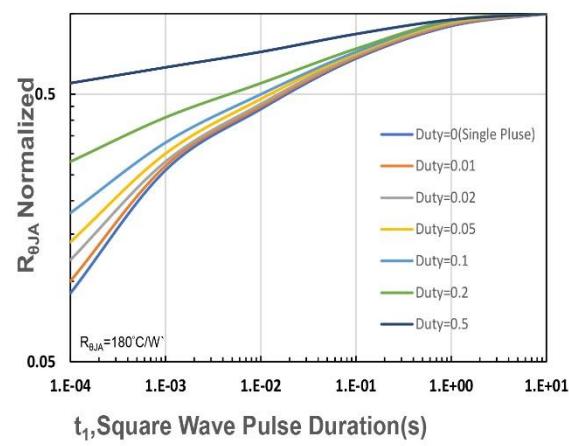


Figure 12. $R_{θJA}$ Transient Thermal Impedance