Power MOSFETS

DATASHEET

LM30120DAK8A

Dual N-Channel

Enhancement Mode MOSFET

Leadpower-semiconductor Corp., Ltd

sales@leadpower-semi.com

(03) 6577339　FAX：(03) 6577229

www.leadpower-semi.com

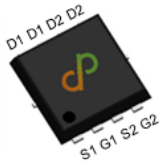
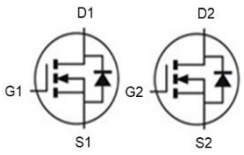
Quality Management Systems

ISO 9001:2015 Certificate

LM30120DAK8A

Dual N-Channel Enhancement Mode MOSFET

Pin Description

PDFN5*6 (TOP view)	Symbol
	

Product Summary

Symbol	Dual N-Channel	Unit
V_{DSS}	30	V
$R_{DS(ON)-Max}$	12	mΩ
ID	30	A

Feature

- Fast switching speed
- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- 100% UIS and Rg Tested

Applications

- DC-DC Converters
- Portable equipment application

Ordering Information

Orderable Part Number	Package Type	Form	Shipping
LM30120DAK8A	PDFN5*6(Dual)	Tape & Reel	5000 / Tape & Reel

Absolute Maximum Ratings (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter		Dual N-Channel	Unit
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		±20	
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature Range		-55 to 150	°C
I_{DM}①	Pulse Drain Current Tested	T_C=25°C	38	A
I_D	Continuous Drain Current	T_C=25°C	30	A
		T_C=100°C	19	
P_D	Maximum Power Dissipation	T_C=25°C	18	W
		T_C=100°C	7	
I_{AS}②	Avalanche Current, Single pulse	L=0.1mH	18	A
E_{AS}②	Avalanche Energy, Single pulse	L=0.1mH	16	mJ

Thermal Characteristics

Symbol	Parameter		Rating	Unit
$R_{\theta JC}$	Thermal Resistance-Junction to Case	Steady State	7	°C/W
$R_{\theta JA}$③	Thermal Resistance-Junction to Ambient	Steady State	100	°C/W

Note ①：Max. current is limited by bonding wire

Note ②：UIS tested and pulse width are limited by maximum junction temperature 150°C

Note ③：Surface Mounted on 1in^2 FR-4 board with 1oz.

Dual N-Channel Electrical Characteristics (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Electrical Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_{DS}=250uA	30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=24V, V_{GS}=0V	-	-	1	uA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_{DS}=250uA	1.1	1.6	2.1	V
I_{GSS}	Gate Leakage Current	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
$R_{DS(ON)}$④	Drain-Source On-state Resistance	V_{GS}=10V, I_{DS}=10A	-	10	12	mΩ
		V_{GS}=4.5V, I_{DS}=6A	-	12	16	
gfs	Forward Transconductance	V_{DS}=5V, I_{DS}=5A	-	2.5	-	S
Dynamic Characteristics ⑤						
R_G	Gate Resistance	V_{GS}=0V,V_{DS}=0V, Freq.=1MHz	-	3	-	Ω
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, Freq.=1MHz	-	872	-	pF
C_{oss}	Output Capacitance		-	112	-	
C_{rss}	Reverse Transfer Capacitance		-	104	-	
$td_{(ON)}$	Turn-on Delay Time	V_{GS}=10V,V_{DS}=15V, I_D=1A,R_{GEN}=6Ω	-	17	-	nS
t_r	Turn-on Rise Time		-	30	-	
$t_{d(OFF)}$	Turn-off Delay Time		-	30	-	
t_f	Turn-off Fall Time		-	16	-	
Q_g	Total Gate Charge	V_{GS}=4.5V,V_{DS}=15V I_D=10A	-	10.3	-	nC
Q_g	Total Gate Charge	V_{GS}=10V,V_{DS}=15V, I_D=10A	-	20.5	-	
Qgs	Gate-Source Charge		-	2.32	-	
Qgd	Gate-Drain Charge		-	4.8	-	
Source-Drain Characteristics						
V_{SD}④	Diode Forward Voltage	I_{SD}=1A, V_{GS}=0V	-	0.7	1.1	V
t_{rr}	Reverse Recovery Time	I_F=1A, V_R=20V dI$_F$/dt=100A/μs	-	25.4	-	nS
Q_{rr}	Reverse Recovery Charge		-	10.7	-	nC

Note ④：Pulse test (pulse width≤300us, duty cycle≤2%).
Note ⑤：Guaranteed by design, not subject to production testing.

Dual N-Channel Typical Characteristics

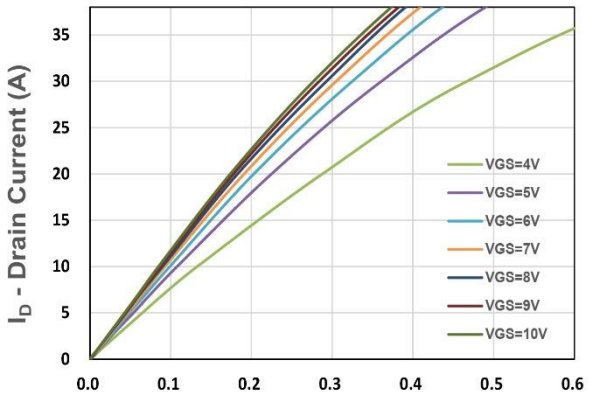


Figure 1. Output Characteristics

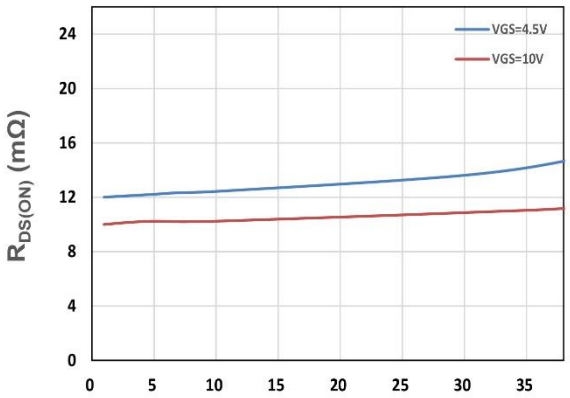


Figure 2. On-Resistance vs. ID

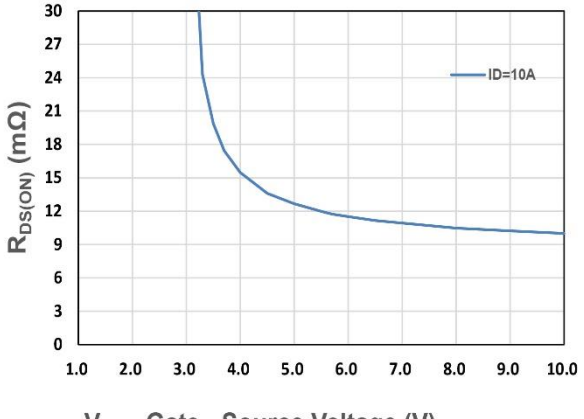


Figure 3. On-Resistance vs. VGS

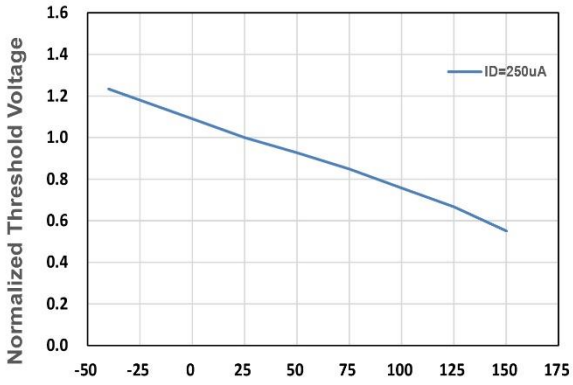


Figure 4. Gate Threshold Voltage

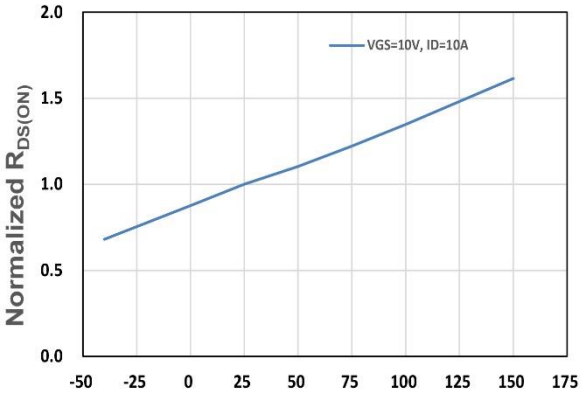


Figure 5. Drain-Source On Resistance

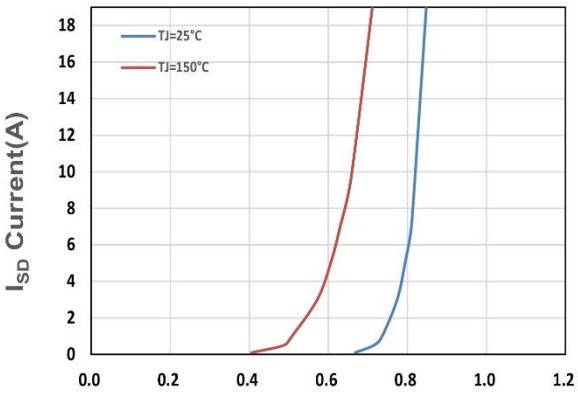
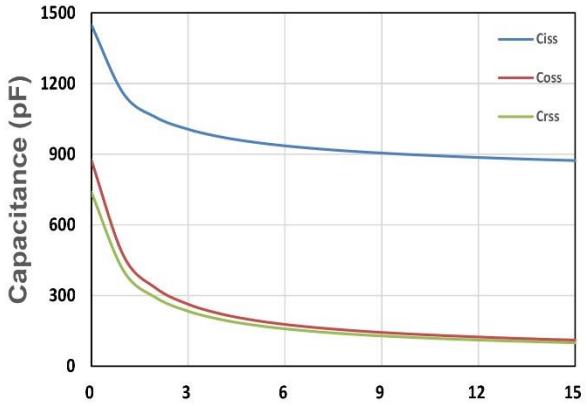
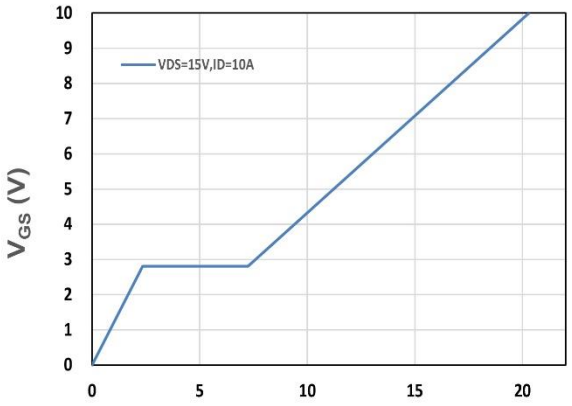


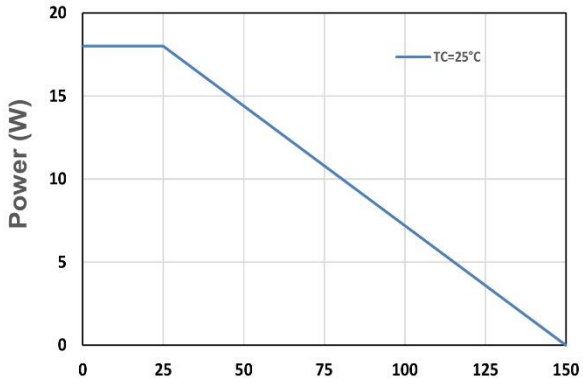
Figure 6. Source-Drain Diode Forward



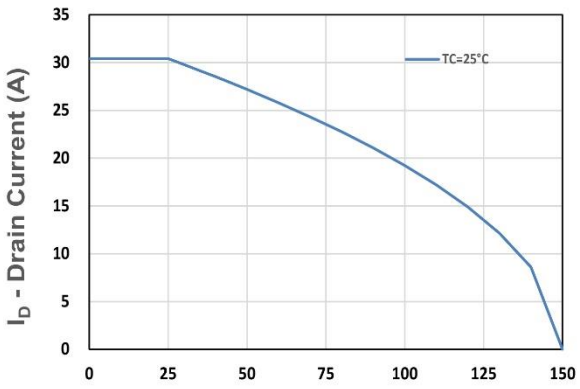
V_{DS} - Drain - Source Voltage (V)
Figure 7. Capacitance



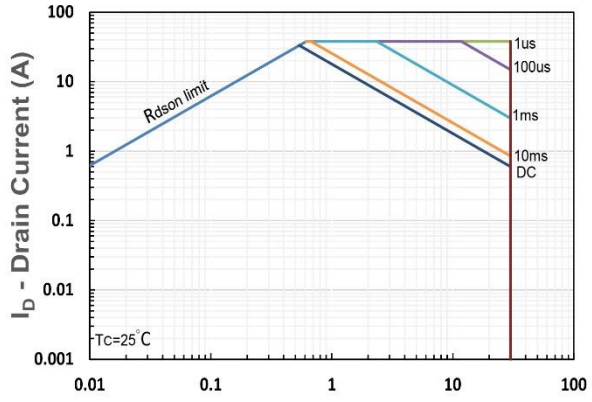
Qg, Total Gate Charge (nC)
Figure 8. Gate Charge Characteristics



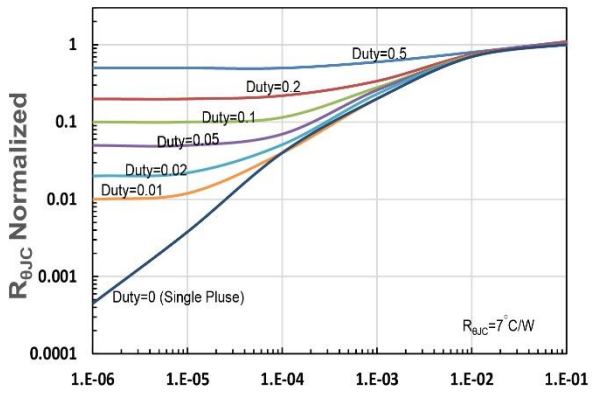
Tj - Junction Temperature (°C)
Figure 9. Power Dissipation



Tj - Junction Temperature (°C)
Figure 10. Drain Current



V_{DS} - Drain-Source Voltage (V)
Figure 11. Safe Operating Area



t_1,Square Wave Pulse Duration(s)
Figure 12. RθJC Transient Thermal Impedance