Power MOSFETS

DATASHEET

LM30160TAQ8A

Dual P-Channel

Enhancement Mode MOSFET

Leadpower-semiconductor Corp., Ltd

sales@leadpower-semi.com

(03) 6577339　FAX：(03) 6577229

www.leadpower-semi.com

Quality Management Systems

ISO 9001:2015 Certificate

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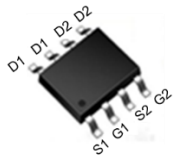
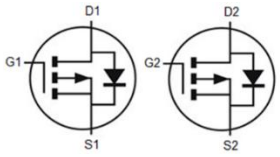
Pin Description

SOP-8L(Dual) (TOP view)



Symbol



Ordering Information

Symbol	Dual P-Channel	Unit
V_{DSS}	**-30**	**V**
$R_{DS(ON)-Max}$	**18**	**mΩ**
I_D	**-7.3**	**A**

Feature

- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- Lower Qg and Qgd for high-speed switching
- Lower RDS(ON) to Minimize Conduction Losses
- 100% UIS Tested

Applications

- Power Management in DC/DC
- Power Load Switch

Ordering Information

Orderable Part Number	Package Type	Form	Shipping
LM30160TAQ8A	SOP-8L(Dual)	Tape & Reel	3000 / Tape & Reel

Absolute Maximum Ratings (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter		Dual P-Channel	Unit
V_{DSS}	Drain-Source Voltage		-30	V
V_{GSS}	Gate-Source Voltage		±25	
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature Range		-55 to 150	°C
I_{DM}①	Pulse Drain Current Tested	T_A=25°C	-18	A
I_D③	Continuous Drain Current	T_A=25°C	-7.3	A
		T_A=70°C	-5.8	
P_D③	Maximum Power Dissipation	T_A=25°C	1.5	W
		T_A=70°C	0.9	
I_{AS}③	Avalanche Current, Single pulse	L=0.1mH	-18	A
E_{AS}②	Avalanche Energy, Single pulse	L=0.1mH	16	mJ

Thermal Characteristics

Symbol	Parameter		Rating	Unit
$R_{\theta JA}$③	Thermal Resistance-Junction to Ambient	t<=10s	44	°C/W
		Steady State	85	°C/W

Note ① : Max. current is limited by junction temperature.
Note ② : UIS tested and pulse width are limited by maximum junction temperature 150°C
Note ③ : Surface Mounted on 1in² FR-4 board with 1oz.

Dual P-Channel Electrical Characteristics (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Electrical Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_{DS}=-250uA	-30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-24V, V_{GS}=0V	-	-	-1	uA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_{DS}=-250uA	-1	-1.5	-2	V
I_{GSS}	Gate Leakage Current	V_{GS}=±25V, V_{DS}=0V	-	-	±100	nA
$R_{DS(ON)}$④	Drain-Source On-state Resistance	V_{GS}=-10V, I_{DS}=-10A	-	15	18	mΩ
		V_{GS}=-4.5V, I_{DS}=-7A	-	18	23	
gfs	Forward Transconductance	V_{DS}=-10V, I_{DS}=-5A	-	14.7	-	S
Dynamic Characteristics ⑤						
R_G	Gate Resistance	V_{GS}=0V,V_{DS}=0V, Freq.=1MHz	-	8.9	-	Ω
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-15V, Freq.=1MHz	-	2157	-	pF
C_{oss}	Output Capacitance		-	235	-	
C_{rss}	Reverse Transfer Capacitance		-	206	-	
$td_{(ON)}$	Turn-on Delay Time	V_{GS}=-10V,V_{DS}=-15V, I_D=-1A,R_{GEN}=6Ω	-	10.6	-	nS
t_r	Turn-on Rise Time		-	15.6	-	
$t_{d(OFF)}$	Turn-off Delay Time		-	90	-	
t_f	Turn-off Fall Time		-	31.2	-	
Q_g	Total Gate Charge	V_{GS}=-4.5V,V_{DS}=-15V I_D=-10A	-	23	-	nC
Q_g	Total Gate Charge	V_{GS}=-10V,V_{DS}=-15V, I_D=-10A	-	46	-	
Qgs	Gate-Source Charge		-	6.5	-	
Qgd	Gate-Drain Charge		-	8.8	-	
Source-Drain Characteristics						
V_{SD}④	Diode Forward Voltage	I_{SD}=-5A, V_{GS}=0V	-	-0.75	-1.1	V
t_{rr}	Reverse Recovery Time	I_F=-5A, V_R=-15V, dI_F/dt=1A/μs	-	13.4	-	nS
Q_{rr}	Reverse Recovery Charge		-	7.1	-	nC

Note ④：Pulse test (pulse width≤300us, duty cycle≤2%).
Note ⑤：Guaranteed by design, not subject to production testing.

Dual P-Channel Typical Characteristics

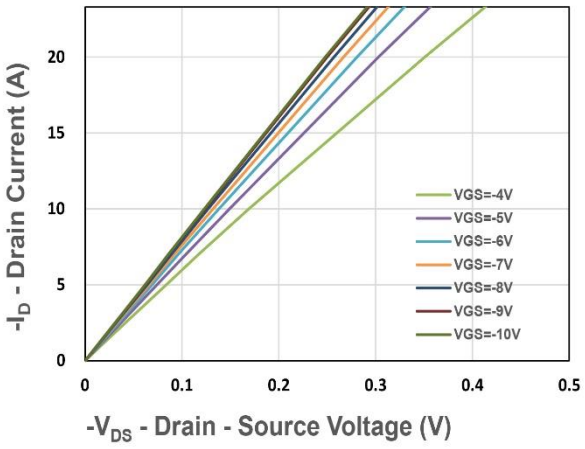


Figure 1. Output Characteristics

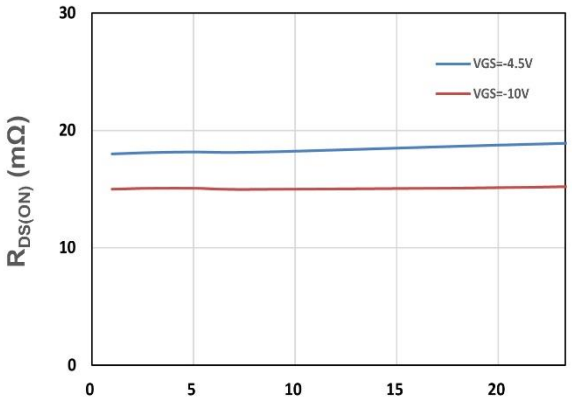


Figure 2. On-Resistance vs. ID

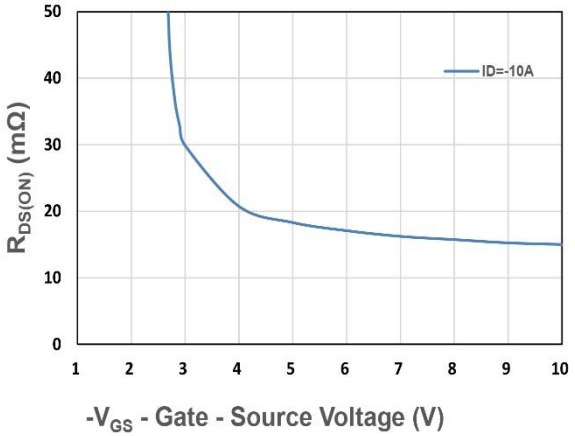


Figure 3. On-Resistance vs. VGS

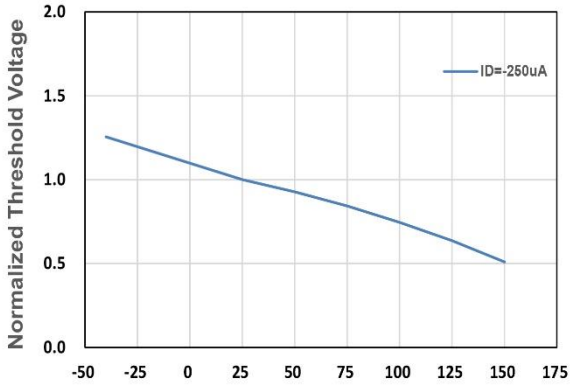


Figure 4. Gate Threshold Voltage

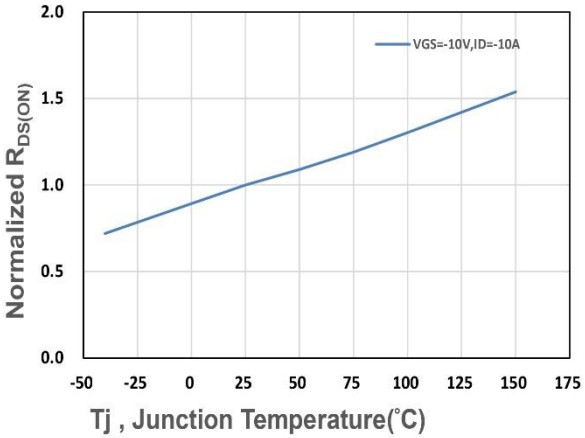


Figure 5. Drain-Source On Resistance

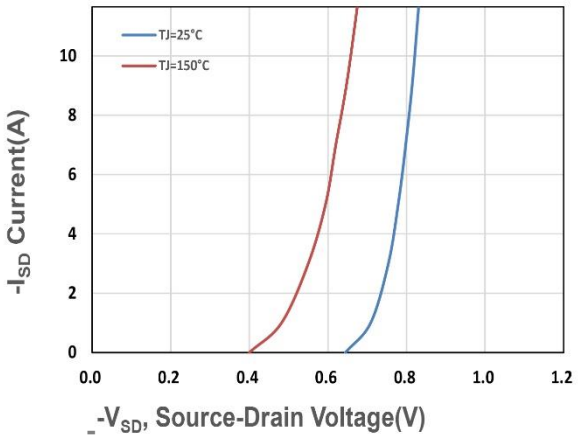


Figure 6. Source-Drain Diode Forward

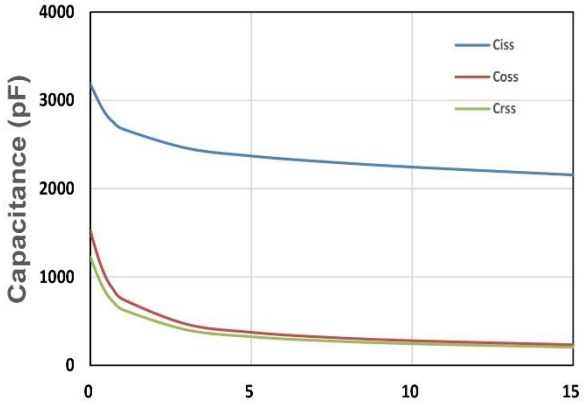


Figure 7. Capacitance

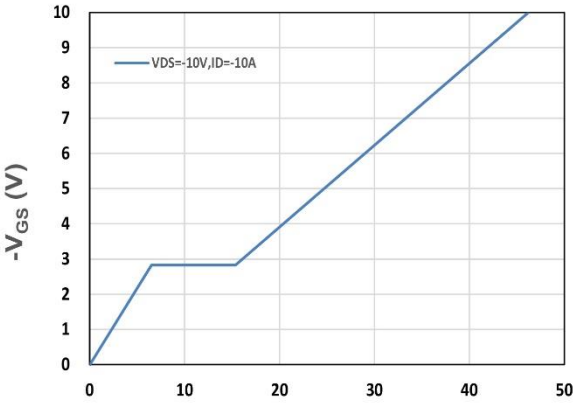


Figure 8. Gate Charge Characteristics

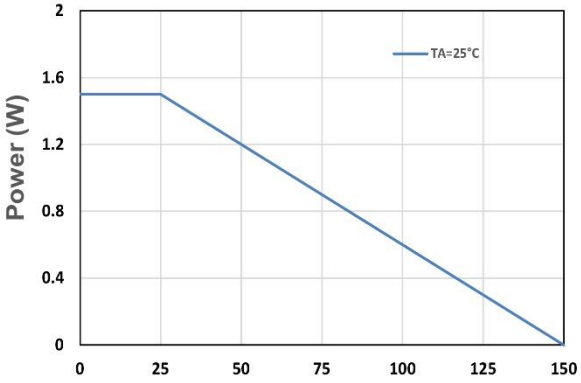


Figure 9. Power Dissipation

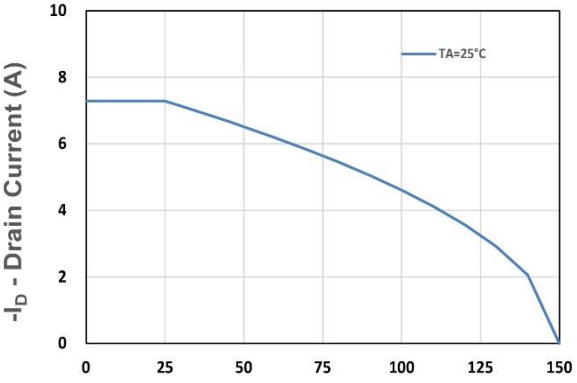


Figure 10. Drain Current

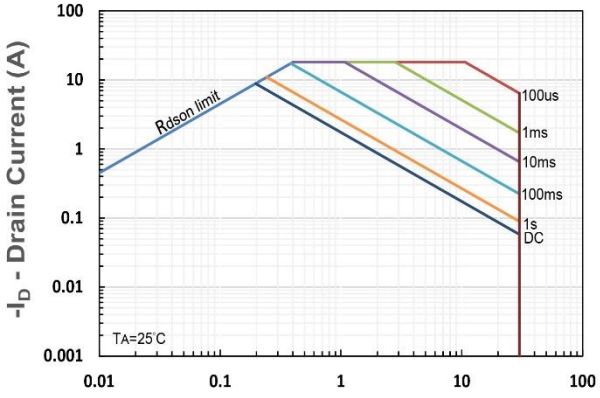


Figure 11. Safe Operating Area

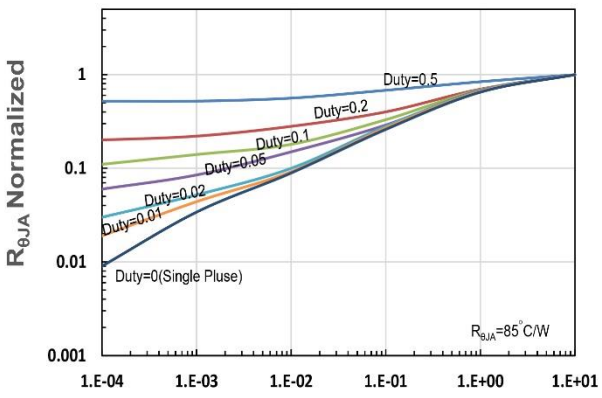


Figure 12. RθJA Transient Thermal Impedance