



Power MOSFETS

DATASHEET

LM40030NAK8A

N-Channel
Enhancement Mode MOSFET

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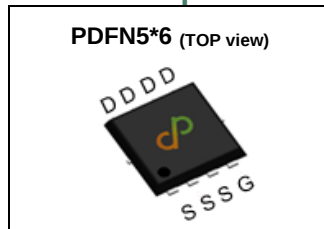


Quality Management Systems

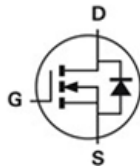
ISO 9001:2015 Certificate

N-Channel Enhancement Mode MOSFET

Pin Description



Symbol



Product Summary

Symbol	N-Channel	Unit
V_{DS}	40	V
$R_{DS(ON)-Max}$	3	m Ω
ID	142	A

Feature

- Ultra low Rdson and low parasitic inductance
- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- 100% UIS and Rg Tested

Applications

- DC-to-DC converters
- Server power supplier

Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM40030NAK8A	PDFN5*6	Tape & Reel	5000 / Tape & Reel	40030 □□□□□G

Absolute Maximum Ratings ($T_J=25^\circ\text{C}$ Unless Otherwise Noted)

Symbol	Parameter		N-Channel	Unit
V_{DS}	Drain-Source Voltage		40	V
V_{GS}	Gate-Source Voltage		± 20	
T_J	Maximum Junction Temperature		150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range		-55 to 150	$^\circ\text{C}$
$I_{DM}^{①}$	Pulse Drain Current Tested	$T_C=25^\circ\text{C}$	142	A
I_D	Continuous Drain Current	$T_C=25^\circ\text{C}$	142 ^①	A
		$T_C=100^\circ\text{C}$	92	
P_D	Maximum Power Dissipation	$T_C=25^\circ\text{C}$	87	W
		$T_C=100^\circ\text{C}$	35	
$I_{AS}^{②}$	Avalanche Current, Single pulse	$L=0.1\text{mH}$	37	A
$E_{AS}^{②}$	Avalanche Energy, Single pulse	$L=0.1\text{mH}$	68	mJ

Thermal Characteristics

Symbol	Parameter		Rating	Unit
$R_{\theta JC}$	Thermal Resistance-Junction to Case	Steady State	1.44	$^\circ\text{C/W}$
$R_{\theta JA}^{③}$	Thermal Resistance-Junction to Ambient	Steady State	65	$^\circ\text{C/W}$

Note ① : Max. current is limited by bonding wire

Note ② : UIS tested and pulse width are limited by maximum junction temperature 150°C

Note ③ : Surface Mounted on 1in^2 FR-4 board with 1oz.

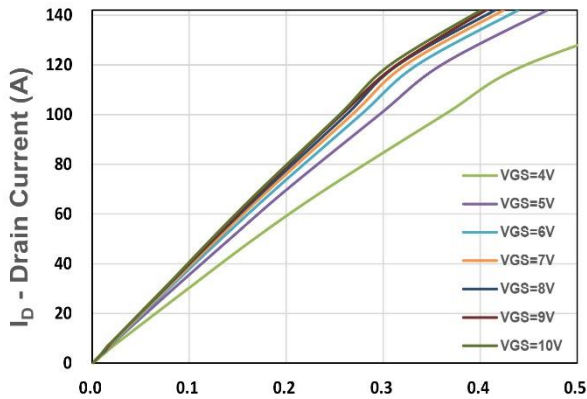
N-Channel Electrical Characteristics ($T_J=25^{\circ}\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Electrical Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =250uA	40	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =32V, V _{GS} =0V	-	-	1	uA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =250uA	1	1.5	2	V
I _{GSS}	Gate Leakage Current	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
R _{DS(ON)} ④	Drain-Source On-state Resistance	V _{GS} =10V, I _{DS} =20A	-	2.4	3	mΩ
		V _{GS} =4.5V, I _{DS} =15A	-	2.9	3.8	
gfs	Forward Transconductance	V _{DS} =5V, I _{DS} =10A	-	46.4	-	S
Dynamic Characteristics ⑥						
R _G	Gate Resistance	V _{GS} =0V, V _{DS} =0V, Freq.=1MHz	-	1.6	-	Ω
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =20V, Freq.=1MHz	-	5451	-	pF
C _{oss}	Output Capacitance		-	484	-	
C _{rss}	Reverse Transfer Capacitance		-	406	-	
td(ON)	Turn-on Delay Time	V _{GS} =10V, V _{DS} =25V, I _D =1A, R _{GEN} =6Ω	-	20.8	-	nS
t _r	Turn-on Rise Time		-	26.2	-	
t _{d(OFF)}	Turn-off Delay Time		-	213.1	-	
t _f	Turn-off Fall Time		-	81.8	-	
Q _g	Total Gate Charge	V _{GS} =4.5V, V _{DS} =20V I _D =20A	-	77.3	-	nC
Q _g	Total Gate Charge	V _{GS} =10V, V _{DS} =20V, I _D =20A	-	156.7	-	
Q _{gs}	Gate-Source Charge		-	29.4	-	
Q _{gd}	Gate-Drain Charge		-	26	-	
Source-Drain Characteristics						
V _{SD} ④	Diode Forward Voltage	I _{SD} =10A, V _{GS} =0V	-	0.7	1.1	V
t _{rr}	Reverse Recovery Time	I _F =10A, V _R =20V	-	31.2	-	nS
Q _{rr}	Reverse Recovery Charge	dI _F /dt=100A/μs	-	32.1	-	nC

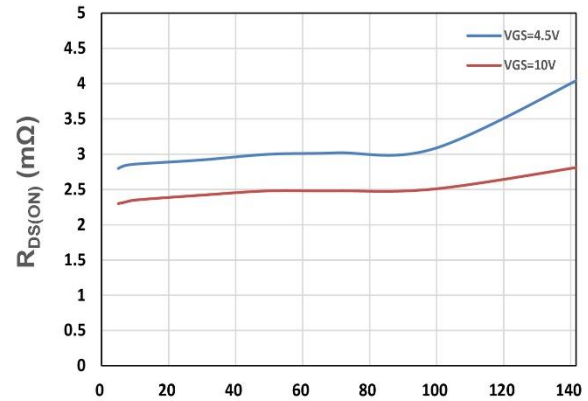
Note ④ : Pulse test (pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$).

Note ⑤ : Guaranteed by design, not subject to production testing.

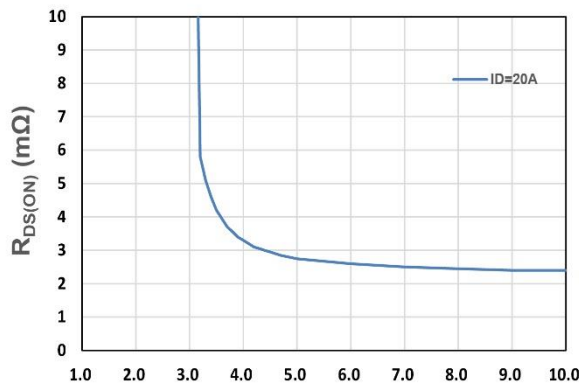
N-Channel Typical Characteristics



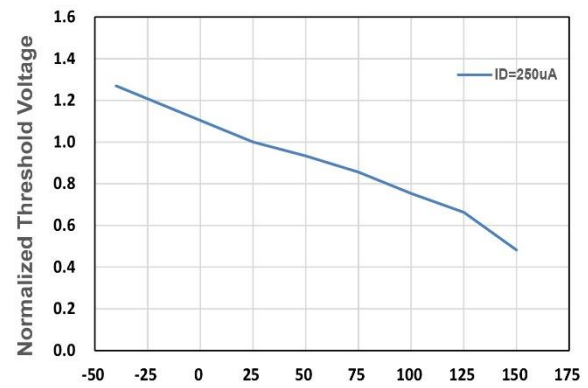
V_{DS} - Drain - Source Voltage (V)
Figure 1. Output Characteristics



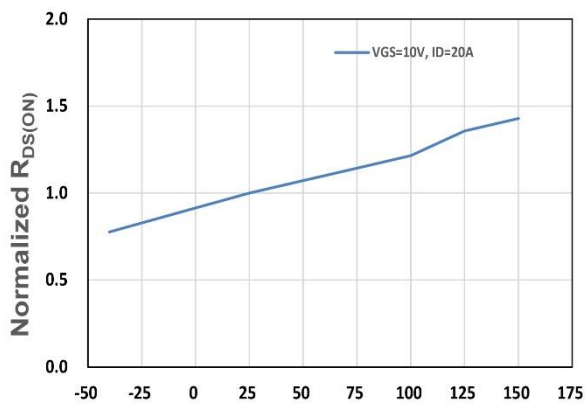
I_D - Drain Current (A)
Figure 2. On-Resistance vs. I_D



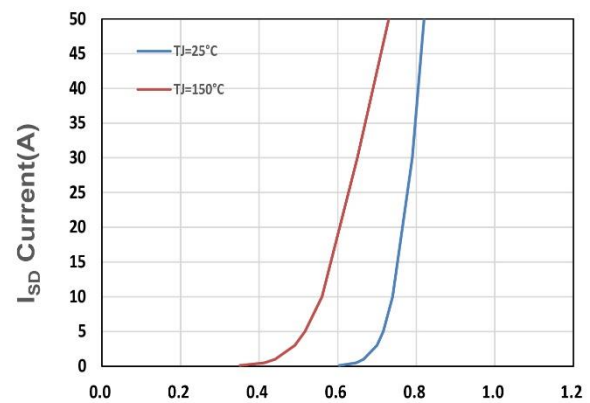
V_{GS} - Gate - Source Voltage (V)
Figure 3. On-Resistance vs. V_{GS}



T_j , Junction Temperature($^{\circ}C$)
Figure 4. Gate Threshold Voltage



T_j , Junction Temperature($^{\circ}C$)
Figure 5. Drain-Source On Resistance



V_{SD} , Source-Drain Voltage(V)
Figure 6. Source-Drain Diode Forward

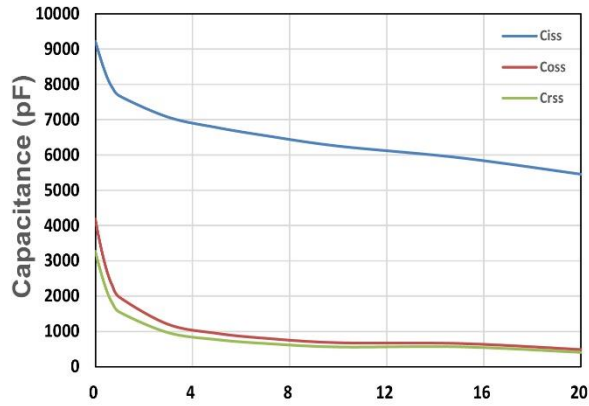


Figure 7. Capacitance

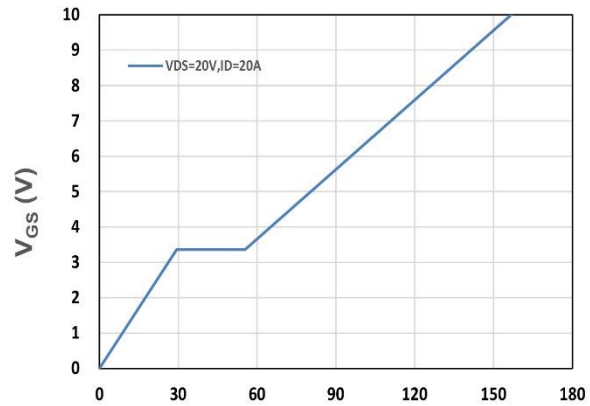


Figure 8. Gate Charge Characteristics

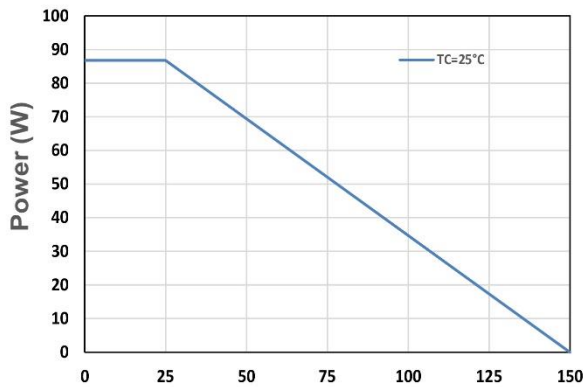


Figure 9. Power Dissipation

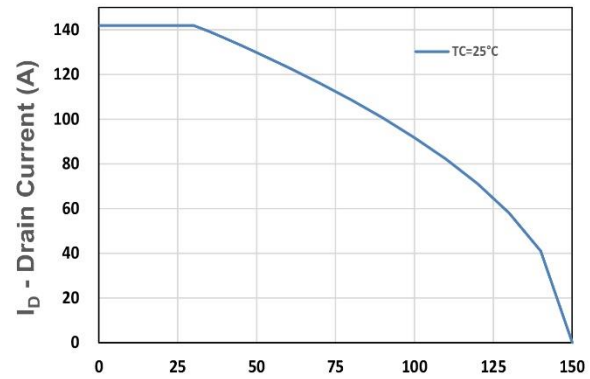


Figure 10. Drain Current

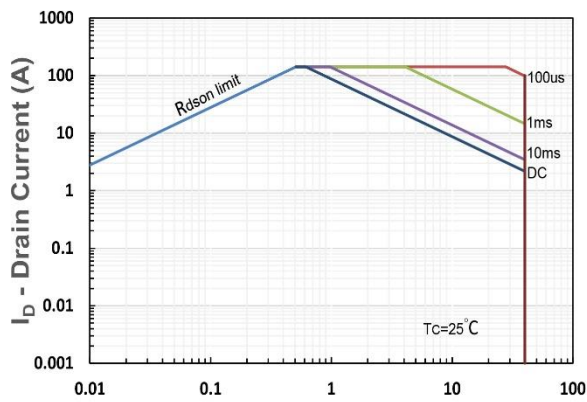


Figure 11. Safe Operating Area

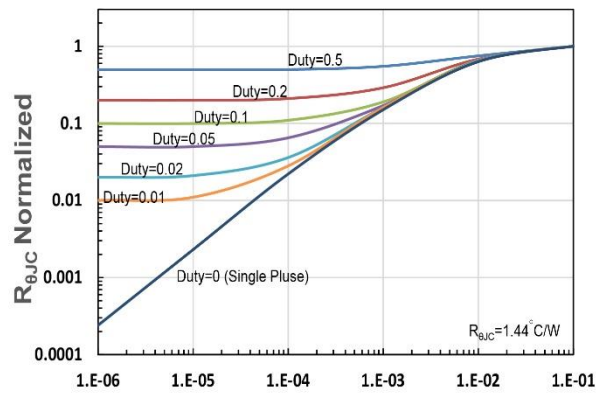


Figure 12. $R_{\theta JC}$ Transient Thermal Impedance