



Power MOSFETS

DATASHEET

LM40068NAI8A

N-Channel
Enhancement Mode MOSFET

 Leadpower-semi CO., LTD.

 sales@leadpower-semi.com

 (03) 6577339 FAX : (03) 6577229

 www.leadpower-semi.com

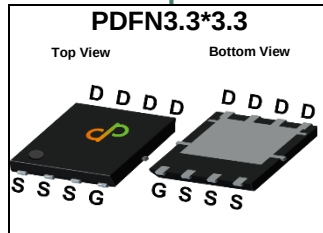


Quality Management Systems

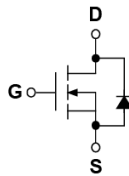
ISO 9001:2015 Certificate

N-Channel Enhancement Mode MOSFET

Pin Description



Symbol



Product Summary

Symbol	N-Channel	Unit
V_{DSS}	40	V
$R_{DS(ON)-Max}$	7	m Ω
ID	51	A

Feature

- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- 100% UIS and Rg Tested

Applications

- Power Management in DC/DC Converters

Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM40068NAI8A	PDFN3.3*3.3	Tape & Reel	5000 / Tape & Reel	40068 □□□□□□

Note: □□□□□□ = Lot code

Absolute Maximum Ratings (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter	N-Channel	Unit
V_{DSS}	Drain-Source Voltage	40	V
V_{GSS}	Gate-Source Voltage	±20	V
T_J	Maximum Junction Temperature	175	°C
T_{STG}	Storage Temperature Range	-55 to 175	°C
I_S	Diode Continuous Forward Current	$T_C=25^\circ\text{C}$	20.7
I_{DM}	Pulse Drain Current Tested	$T_C=25^\circ\text{C}$	127 ^①
I_D	Continuous Drain Current	$T_C=25^\circ\text{C}$	51
		$T_C=100^\circ\text{C}$	36
P_D	Maximum Power Dissipation	$T_C=25^\circ\text{C}$	31.9
		$T_C=100^\circ\text{C}$	16
$I_D^{②}$	Continuous Drain Current	$T_A=25^\circ\text{C}$	13.2
		$T_A=70^\circ\text{C}$	11
$P_D^{②}$	Maximum Power Dissipation	$T_A=25^\circ\text{C}$	2.1
		$T_A=70^\circ\text{C}$	1.5
$I_{AS}^{③}$	Avalanche Current, Single pulse	L=0.1mH	16
		L=0.5mH	9
$E_{AS}^{③}$	Avalanche Energy, Single pulse	L=0.1mH	12.8
		L=0.5mH	20

Thermal Characteristics

Symbol	Parameter	Rating	Unit
$R_{\theta JC}$	Thermal Resistance-Junction to Case	Steady State	4.7
$R_{\theta JA}^{②}$	Thermal Resistance-Junction to Ambient	Steady State	70

Note ① : Max. current is limited by junction temperature

Note ② : Surface Mounted on 1in² FR-4 board with 1oz.

Note ③ : UIS tested and pulse width are limited by maximum junction temperature 175°C.

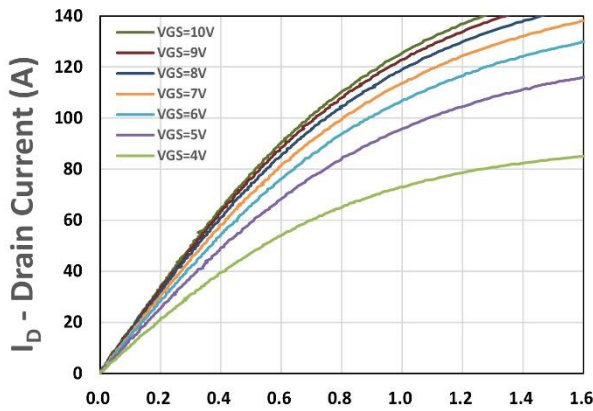
N-Channel Electrical Characteristics ($T_J=25^{\circ}\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Electrical Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =250uA	40	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =32V, V _{GS} =0V	-	-	1	uA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =250uA	1	1.8	2.3	V
I _{GSS}	Gate Leakage Current	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
R _{DS(ON)} ④	Drain-Source On-state Resistance	V _{GS} =10V, I _{DS} =15A	-	5.8	7.0	mΩ
		V _{GS} =4.5V, I _{DS} =6A	-	9.8	12.9	
gfs	Forward Transconductance	V _{DS} =5V, I _{DS} =10A	-	13.9	-	S
Dynamic Characteristics ⑥						
R _G	Gate Resistance	V _{GS} =0V, V _{DS} =0V, Freq.=1MHz	-	2	-	Ω
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =20V, Freq.=1MHz	-	690	-	pF
C _{oss}	Output Capacitance		-	272	-	
C _{rss}	Reverse Transfer Capacitance		-	32	-	
td(ON)	Turn-on Delay Time	V _{GS} =10V, V _{DS} =20V, Id=1A, RGEN=1Ω	-	7	-	nS
tr	Turn-on Rise Time		-	10	-	
td(OFF)	Turn-off Delay Time		-	14	-	
tf	Turn-off Fall Time		-	17	-	
Qg	Total Gate Charge	V _{GS} =4.5V, V _{DS} =20V Id=15A	-	5	-	nC
Qg	Total Gate Charge	V _{GS} =10V, V _{DS} =20V, Id=15A	-	9.9	-	
Qgs	Gate-Source Charge		-	2.8	-	
Qgd	Gate-Drain Charge		-	1.7	-	
Source-Drain Characteristics						
VSD④	Diode Forward Voltage	ISD=20A, VGS=0V	-	0.8	1.1	V
trr	Reverse Recovery Time	IF=7.5A, VR=20V	-	17	-	nS
Qrr	Reverse Recovery Charge	dIF/dt=100A/μs	-	5	-	nC

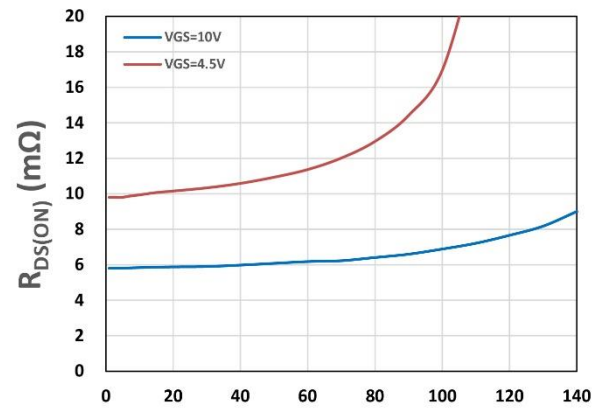
Note ④ : Pulse test (pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$).

Note ⑤ : Guaranteed by design, not subject to production testing.

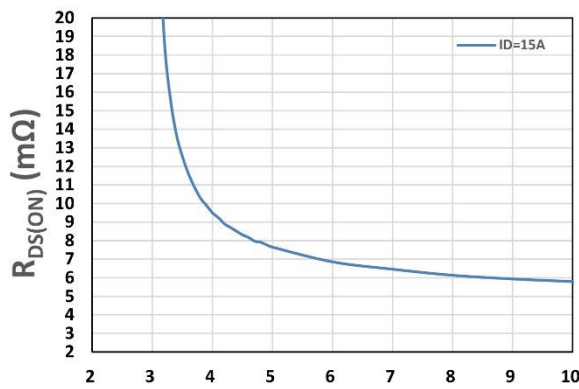
N-Channel Typical Characteristics



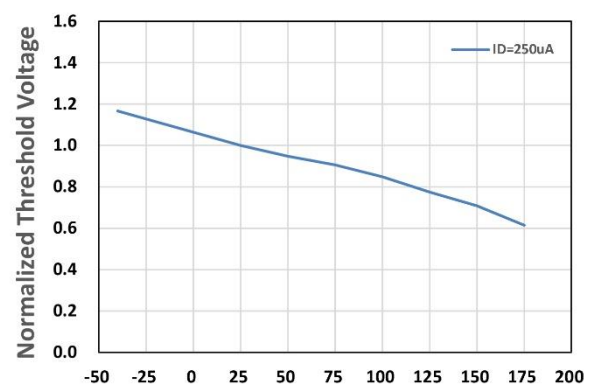
V_{DS} - Drain - Source Voltage (V)
Figure 1. Output Characteristics



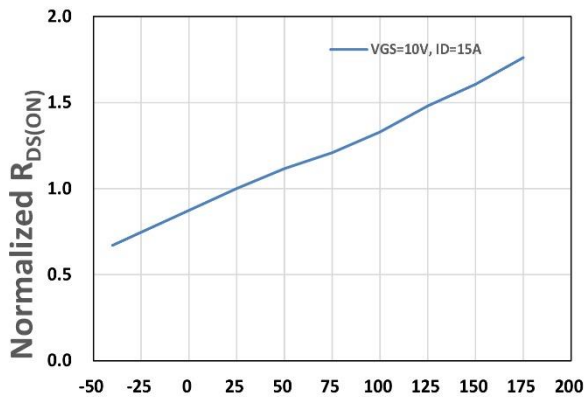
I_D - Drain Current (A)
Figure 2. On-Resistance vs. ID



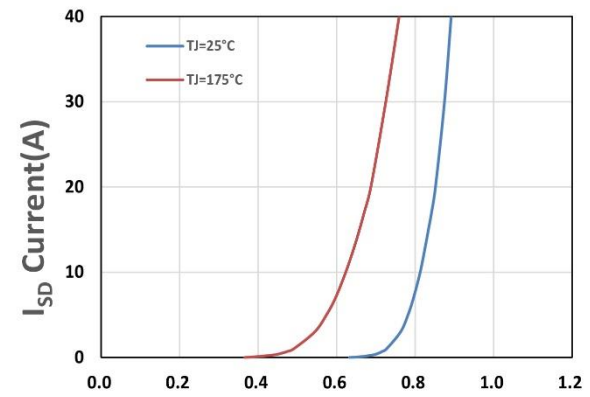
V_{GS} - Gate - Source Voltage (V)
Figure 3. On-Resistance vs. V_{GS}



T_J, Junction Temperature(°C)
Figure 4. Gate Threshold Voltage



T_J, Junction Temperature(°C)
Figure 5. Drain-Source On Resistance



V_{SD}, Source-Drain Voltage(V)
Figure 6. Source-Drain Diode Forward

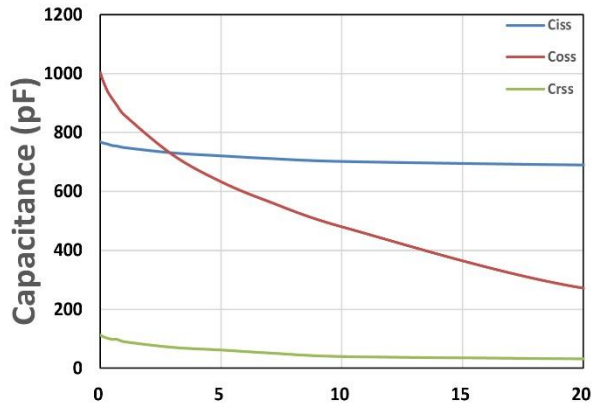


Figure 7. Capacitance

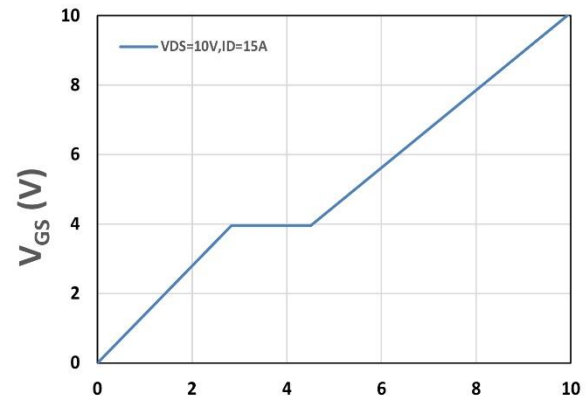


Figure 8. Gate Charge Characteristics

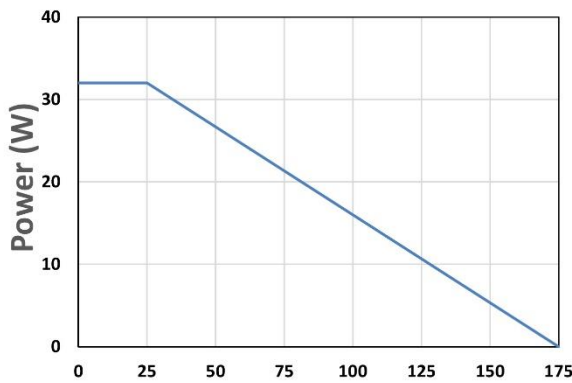


Figure 9. Power Dissipation

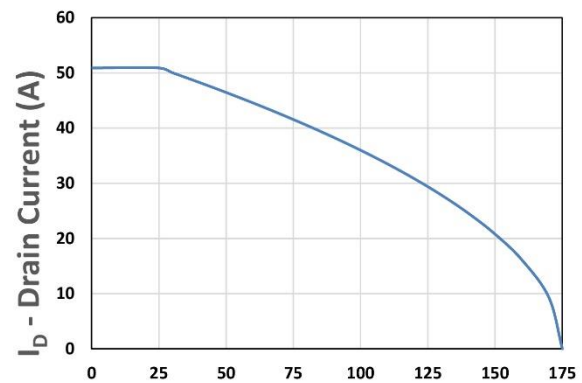


Figure 10. Drain Current

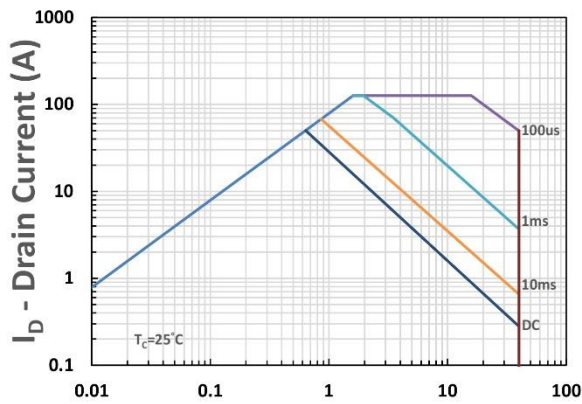


Figure 11. Safe Operating Area

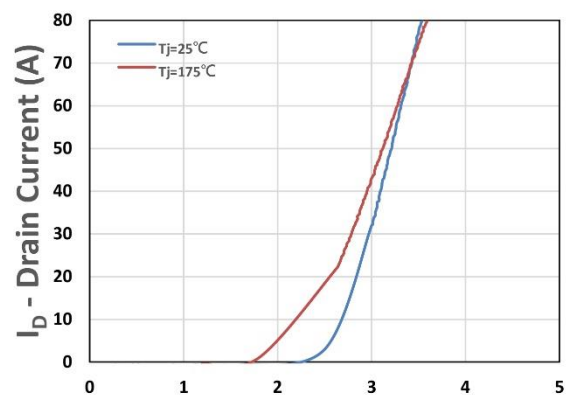


Figure 12. Transfer Characteristics

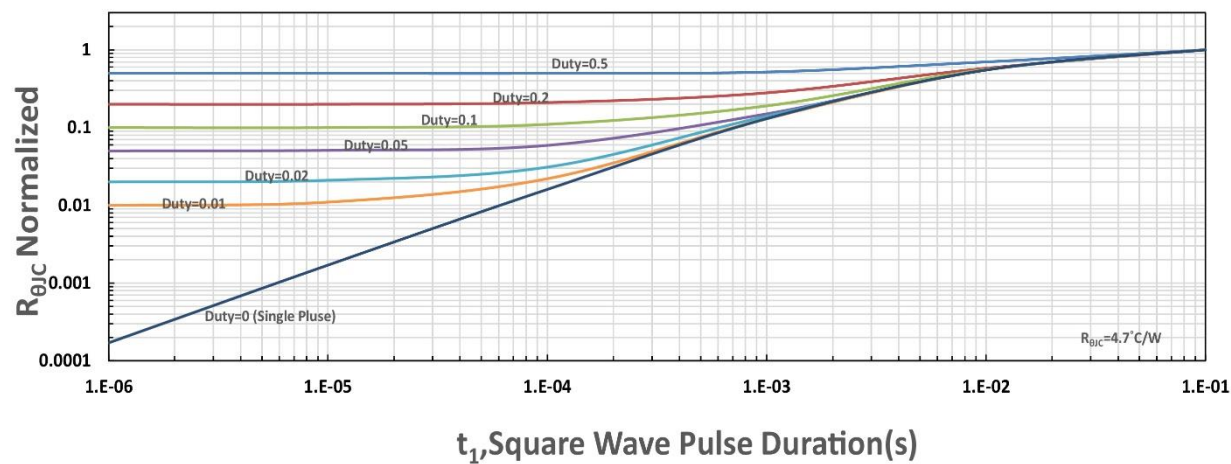


Figure 13. $R_{\theta JC}$ Transient Thermal Impedance