Leadpower
Semiconductor

Power MOSFETS

DATASHEET

LM40068NAK8A

N-Channel
Enhancement Mode MOSFET

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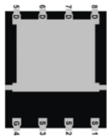
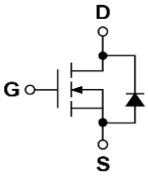
Quality Management Systems

ISO 9001:2015 Certificate

LM40068NAK8A

N-Channel Enhancement Mode MOSFET

▪ Pin Description

	Top view	Bottom view		
PDFN5X6			**Symbol**	

▪ Product Summary

Symbol	N-CH	Unit
V_{DSS}	40	V
$R_{DSON\ (MAX)}$	7.1	mΩ
I_D	55	A

▪ Feature

- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- 100% UIS and Rg Tested

▪ Applications

- Power Management in DC/DC Converters

▪ Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM40068NAK8A	PDFN5X6	Tape & Reel	5000 / Tape & Reel	40068 □□□□□□G

Note：□□□□□ = Lot Code

▪ Absolute Maximum Ratings (T_J=25°C Unless Otherwise Noted)

SYMBOL	PARAMETERS		N-Channel	UNIT
V_{DSS}	Drain-Source Voltage		40	V
V_{GSS}	Gate-Source Voltage		±20	
T_j	Maximum Junction Temperature		175	°C
T_{stg}	Storage Temperature Range		-55 to 175	°C
I_{SP}	Diode Pulse Current[1]	T_C = 25 °C	38	A
I_S	Diode Continuous Forward Current	T_C = 25 °C	15	A
I_{DM}	Pulsed Drain Current[1]		138	A
I_D	Continuous Drain Current	T_C = 25 °C	55	A
		T_C = 100 °C	39	
P_D	Maximum Power Dissipation	T_C = 25 °C	38	W
		T_C = 100 °C	19	
I_D	Continuous Drain Current	T_A = 25 °C	14	A
		T_A = 70 °C	11	
P_D	Maximum Power Dissipation	T_A = 25 °C	2.3	W
		T_A = 70 °C	1.6	
I_{AS}	Avalanche Current,Single pulse[2]	L = 0.1mH	19	A
E_{AS}	Avalanche Energy ,Single pulse[2]	L = 0.1mH	18	mJ
I_{AS}	Avalanche Current,Single pulse[2]	L = 0.5mH	11	A
E_{AS}	Avalanche Energy ,Single pulse[2]	L = 0.5mH	29	mJ

Note ①：Max. current is limited by junction temperature

Note ②：UIS tested and pulse width are limited by maximum junction temperature 175°C

▪ Thermal Characteristics

SYMBOL	PARAMETERS		Rating	UNIT
$R_{\theta JC}$	Thermal Resistance-Junction to Case	Steady State	4	°C / W
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient[3]	Steady State	65	°C / W

▪ N-Channel Electrical Characteristics (T_J=25°C Unless Otherwise Noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Electrical Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	40			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 32V, V_{GS} = 0V			1	μA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	1.2	1.5	2.4	V
I_{GSS}	Gate-Body Leakage	V_{DS} = 0V, V_{GS} = ±20V			±100	nA
$R_{DS(ON)}$	Drain-Source On-State Resistance[4]	V_{GS} = 10V, I_D = 15A		5.8	7.1	mΩ
		V_{GS} = 4.5V, I_D = 6A		10.4	16.5	
g_{fs}	Forward Transconductance	V_{DS} = 5V, I_D = 10A		15		S
Dynamic Characteristics ⑤						
R_g	Gate Resistance	V_{GS}=0V, V_{DS}=0V, f = 1MHz		2.0		Ω
C_{iss}	Input Capacitance	V_{GS} = 0V, V_{DS} = 20V, f = 1MHz		690		pF
C_{oss}	Output Capacitance			272		
C_{rss}	Reverse Transfer Capacitance			32		
$t_{d(on)}$	Turn-On Delay Time	V_{DS} = 20V, V_{GS} = 10V, I_D = 1A , R_{GEN} = 1Ω		7.0		nS
t_r	Turn-On Rise Time			10		
$t_{d(off)}$	Turn-Off Delay Time			14		
t_f	Turn-Off Fall Time			17		
$Q_g(V_{GS}=4.5V)$	Total Gate Charge	V_{DS} = 20V, V_{GS} = 10V, I_D = 15A		5.0		nC
$Q_g(V_{GS}=10V)$	Total Gate Charge			9.9		
Q_{gs}	Gate-Source Charge			2.8		
Q_{gd}	Gate-Drain Charge			1.7		
Source-Drain Characteristics						
V_{SD}	Diode Forward Voltage[4]	I_{SD} = 20A, V_{GS} = 0V		0.84	1.1	V
t_{rr}	Reverse Recovery Time	I_F=20A, V_R=20V dI_F/dt=100A/μs		17		nS
Q_{rr}	Reverse Recovery Charge			5.0		nC

Note ③：Surface Mounted on 1in^2 FR-4 board with 1oz

Note ④：Pulse test (pulse width≦ 300us, duty cycle≦ 2%).

Note ⑤：Guaranteed by design, not subject to production testing.

▪ N-Channel Typical Characteristics

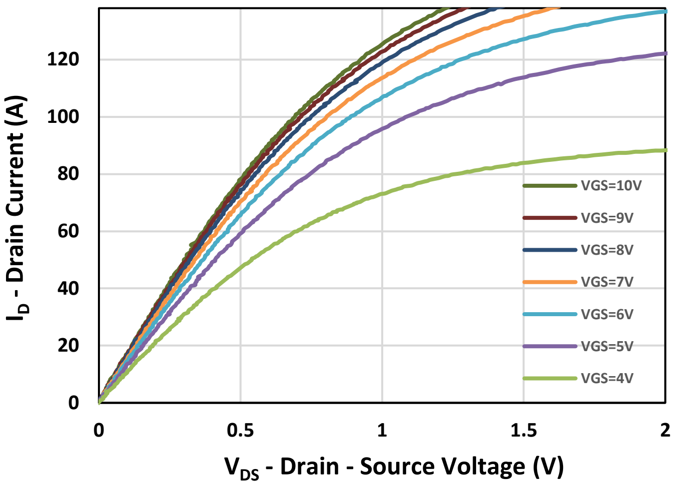


Fig.1 Output Characteristics

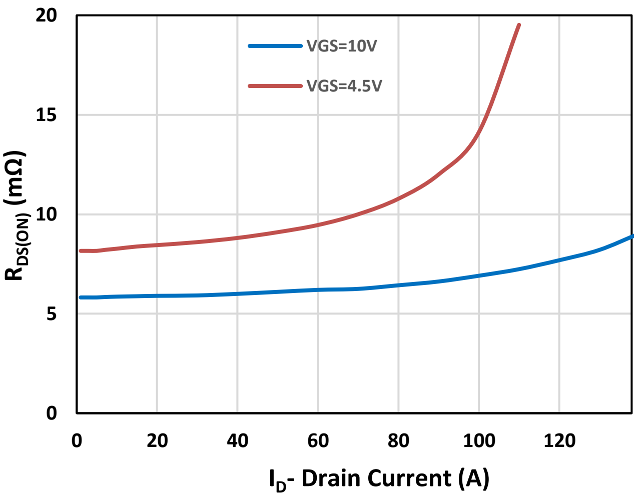


Fig.2 On—Resistance vs. ID

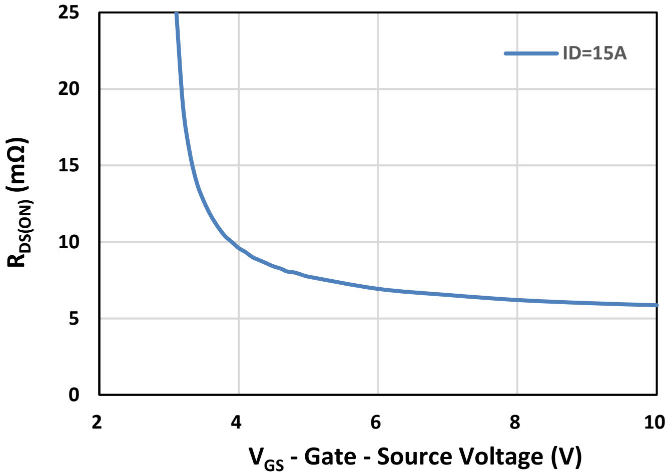


Fig.3 On—Resistance vs. VGS

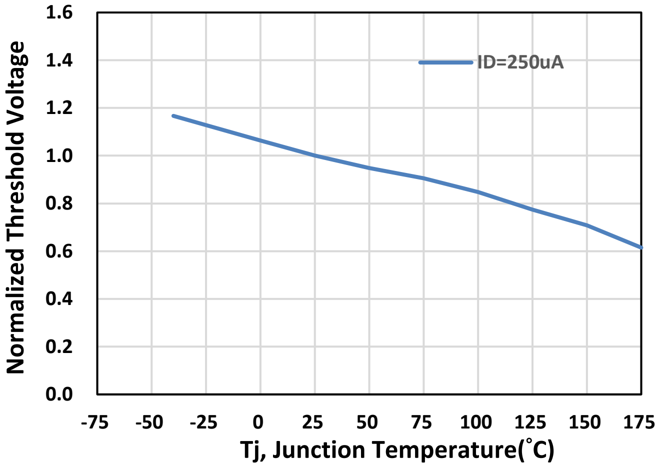


Fig.4 Gate Threshold Voltage

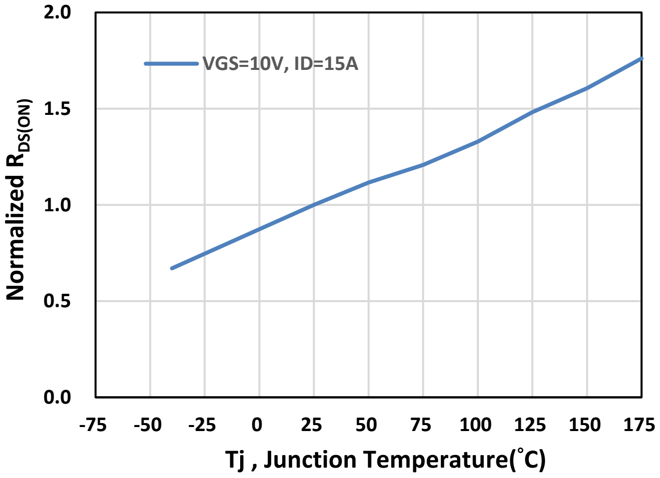


Fig.5 Drain-Source On Resistance

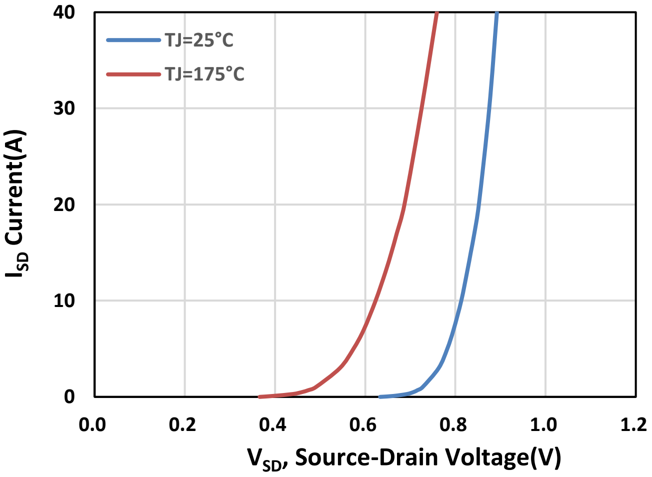


Fig.6 Source-Drain Diode Forward

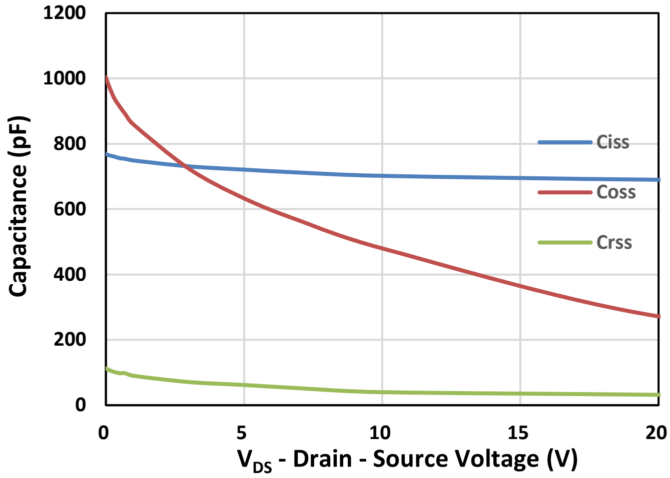


Fig.7 Capacitance

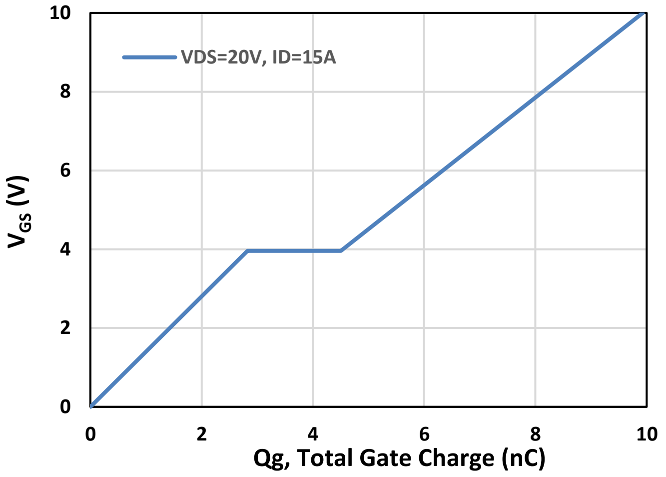


Fig.8 Gate Charge Characteristics

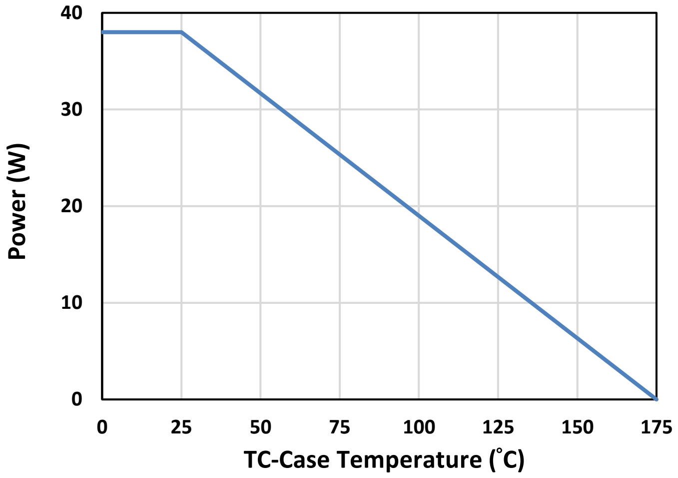


Fig 9. Power dissipation

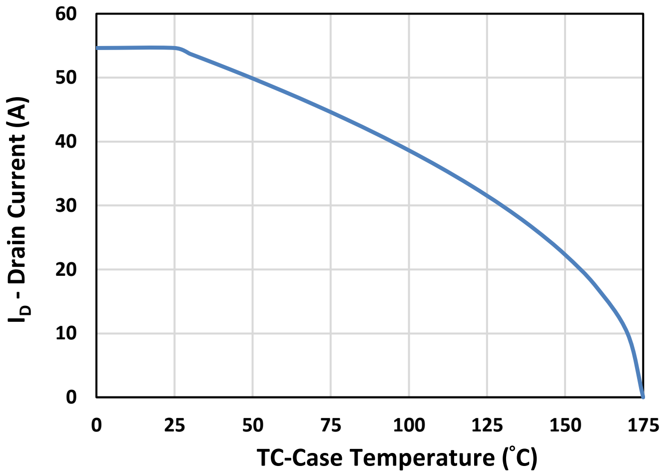


Fig 10. Drain current

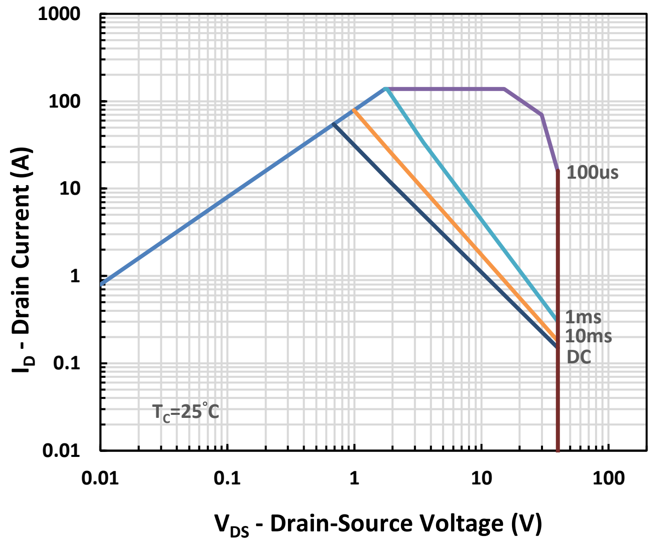


Fig 11. Safe operating area

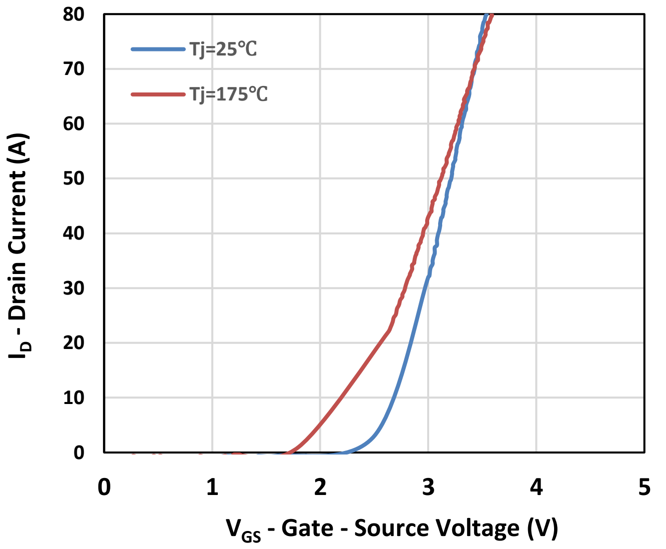


Fig 12. Transfer Characteristics

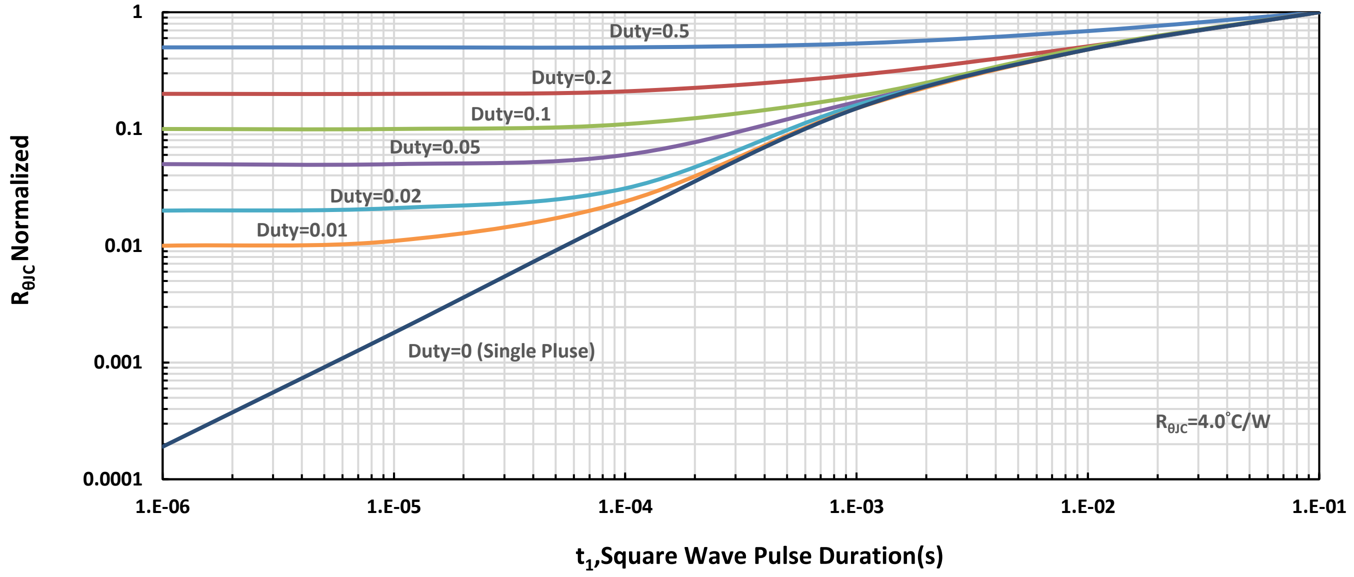


Fig 13. $R_{\theta JC}$ transient thermal impedance