



Power MOSFETS

DATASHEET

LM50J90DEF6A

Dual N-Channel
Enhancement Mode MOSFET

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Quality Management Systems
ISO 9001:2015 Certificate

Dual N-Channel Enhancement Mode MOSFET

Pin Description

SOT-363 (TOP view)	Symbol	Ordering Information												
		<table border="1"> <thead> <tr> <th>Symbol</th> <th>Dual N-Channel</th> <th>Unit</th> </tr> </thead> <tbody> <tr> <td>V_{DSS}</td> <td>50</td> <td>V</td> </tr> <tr> <td>$R_{DS(ON)-Max}$</td> <td>1.9</td> <td>Ω</td> </tr> <tr> <td>I_D</td> <td>0.26</td> <td>A</td> </tr> </tbody> </table>	Symbol	Dual N-Channel	Unit	V_{DSS}	50	V	$R_{DS(ON)-Max}$	1.9	Ω	I_D	0.26	A
Symbol	Dual N-Channel	Unit												
V_{DSS}	50	V												
$R_{DS(ON)-Max}$	1.9	Ω												
I_D	0.26	A												

Feature

- Low V_{th} low gate drive
- ROHS Compliant & Halogen-Free
- ESD protection

Applications

- Small signal application
- Load switch

Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM50J90DEF6A	SOT-363	Tape & Reel	3000 / Tape & Reel	0□□□

Note : □□□= Lot Code

Absolute Maximum Ratings ($T_J=25^\circ\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	Dual N-Channel	Unit
V_{DSS}	Drain-Source Voltage	50	V
V_{GSS}	Gate-Source Voltage	± 20	
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-55 to 150	°C
I_{DM}^{\circledR}	Pulse Drain Current Tested	$T_A=25^\circ\text{C}$	A
I_D	Continuous Drain Current	$T_A=25^\circ\text{C}$	A
		$T_A=70^\circ\text{C}$	
P_D	Maximum Power Dissipation	$T_A=25^\circ\text{C}$	W
		$T_A=70^\circ\text{C}$	

Thermal Characteristics

Symbol	Parameter	Rating	Unit
$R_{\theta JA}^{\circledR}$	Thermal Resistance-Junction to Ambient	500	°C/W

Note ① : Max. current is limited by junction temperature.

Note ② : Surface Mounted on 1in² FR-4 board with 1oz.

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Dual N-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Electrical Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}, I_{\text{DS}}=250\mu\text{A}$	50	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{\text{DS}}=40\text{V}, V_{\text{GS}}=0\text{V}$	-	-	1	μA
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{DS}}=250\mu\text{A}$	0.6	1.2	1.5	V
I_{GSS}	Gate Leakage Current	$V_{\text{GS}}=\pm 20\text{V}, V_{\text{DS}}=0\text{V}$	-	-	± 10	μA
$R_{\text{DS(ON)}}^{\circledast}$	Drain-Source On-state Resistance	$V_{\text{GS}}=10\text{V}, I_{\text{DS}}=0.22\text{A}$	-	1.6	1.9	Ω
		$V_{\text{GS}}=4.5\text{V}, I_{\text{DS}}=0.19\text{A}$	-	1.7	2.2	
		$V_{\text{GS}}=2.5\text{V}, I_{\text{DS}}=0.05\text{A}$	-	2	-	
g_{fs}	Forward Transconductance	$V_{\text{DS}}=3\text{V}, I_{\text{DS}}=0.11\text{A}$	-	0.6	-	S
Dynamic Characteristics ^④						
C_{iss}	Input Capacitance	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=30\text{V}, \text{Freq.}=1\text{MHz}$	-	25	-	pF
C_{oss}	Output Capacitance		-	3.1	-	
C_{rss}	Reverse Transfer Capacitance		-	2.2	-	
$t_{\text{d(ON)}}$	Turn-on Delay Time	$V_{\text{GS}}=10\text{V}, V_{\text{DS}}=50\text{V}, I_{\text{D}}=0.23\text{A}, R_{\text{GEN}}=10\Omega$	-	0.5	-	nS
t_{r}	Turn-on Rise Time		-	19.3	-	
$t_{\text{d(OFF)}}$	Turn-off Delay Time		-	26.3	-	
t_{f}	Turn-off Fall Time		-	22.2	-	
Q_{g}	Total Gate Charge	$V_{\text{GS}}=4.5\text{V}, V_{\text{DS}}=50\text{V}, I_{\text{D}}=1\text{A}$	-	0.91	-	nC
Q_{g}	Total Gate Charge	$V_{\text{GS}}=10\text{V}, V_{\text{DS}}=50\text{V}, I_{\text{D}}=1\text{A}$	-	1.7	-	
Q_{gs}	Gate-Source Charge		-	0.3	-	
Q_{gd}	Gate-Drain Charge		-	0.3	-	
Source-Drain Characteristics						
$V_{\text{SD}}^{\circledast}$	Diode Forward Voltage	$I_{\text{SD}}=0.11\text{A}, V_{\text{GS}}=0\text{V}$	-	0.8	1.1	V
t_{rr}	Reverse Recovery Time	$I_{\text{F}}=0.11\text{A}, V_{\text{GS}}=0$	-	7.2	-	nS
Q_{rr}	Reverse Recovery Charge	$dI_{\text{F}}/dt=100\text{A}/\mu\text{s}$	-	1.9	-	nC

Note ③ : Pulse test (pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$).

Note ④ : Guaranteed by design, not subject to production testing.

Dual N-Channel Typical Characteristics

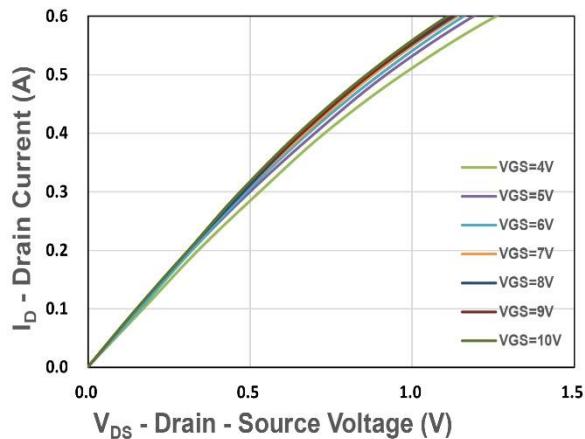


Figure 1. Output Characteristics

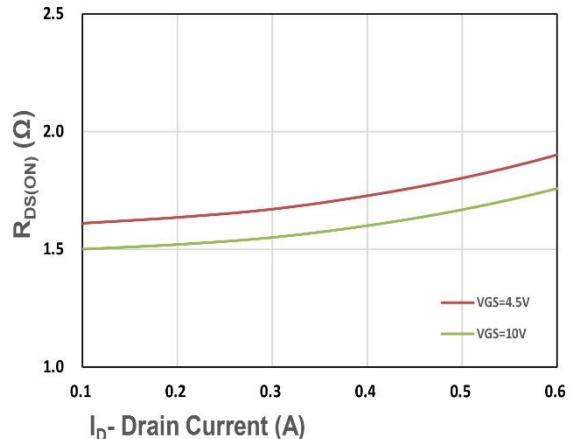


Figure 2. On-Resistance vs. ID

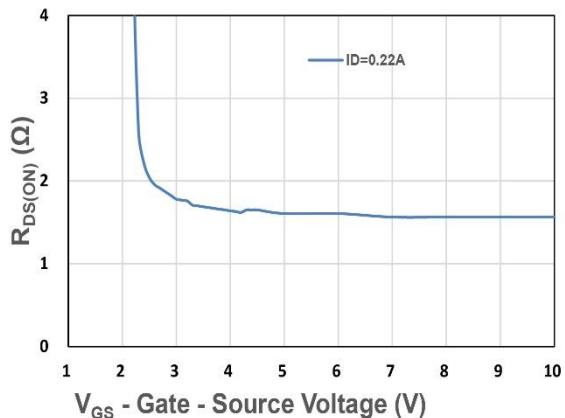


Figure 3. On-Resistance vs. VGS

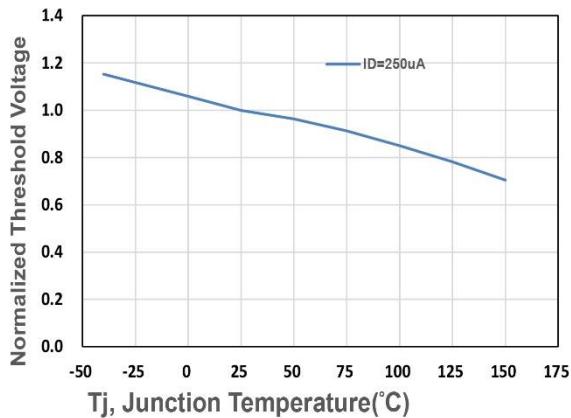


Figure 4. Gate Threshold Voltage

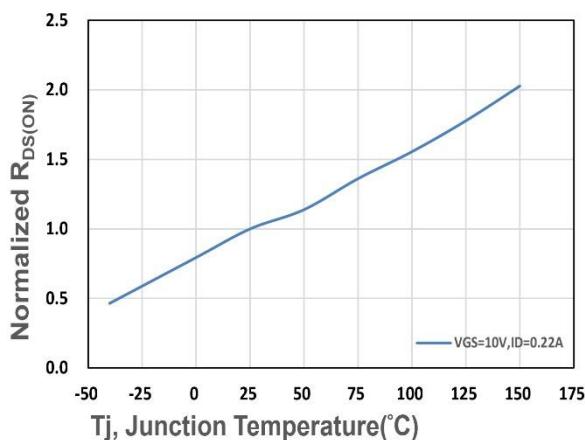


Figure 5. Drain-Source On Resistance

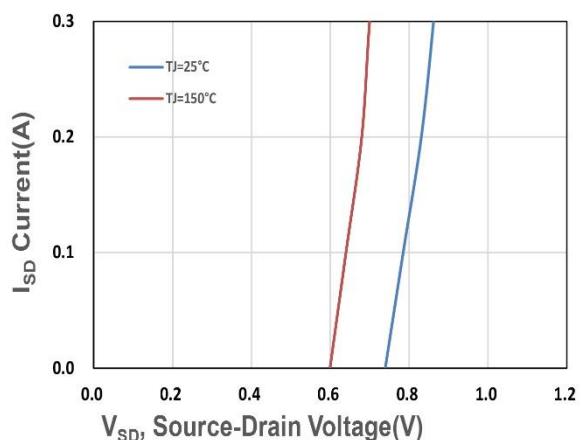


Figure 6. Source-Drain Diode Forward

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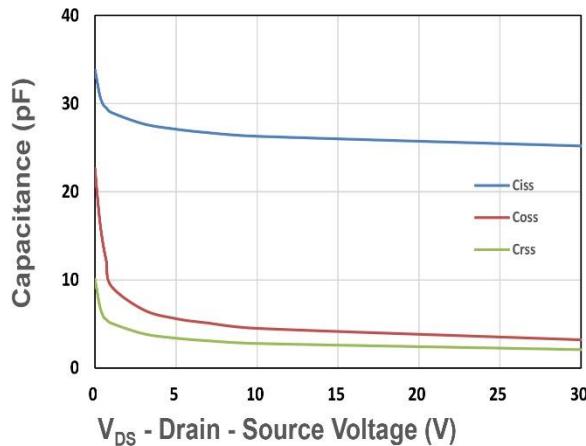


Figure 7. Capacitance

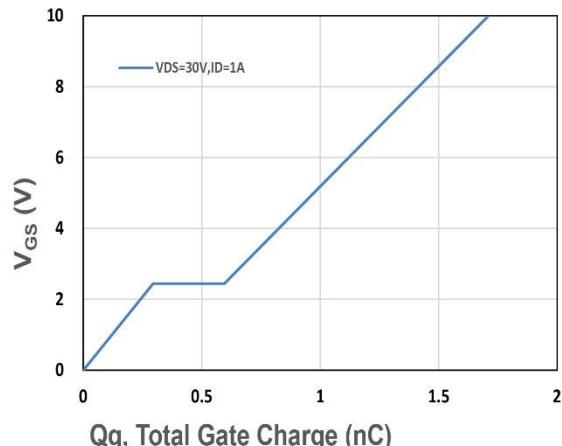


Figure 8. Gate Charge Characteristics

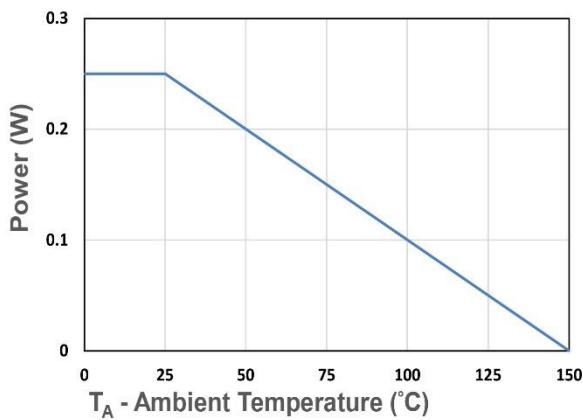


Figure 9. Power Dissipation

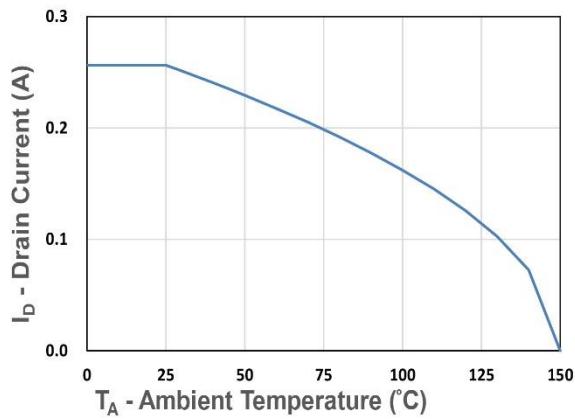


Figure 10. Drain Current

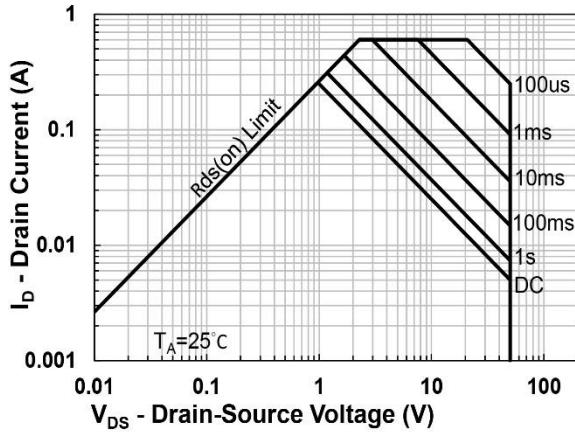


Figure 11. Safe Operating Area

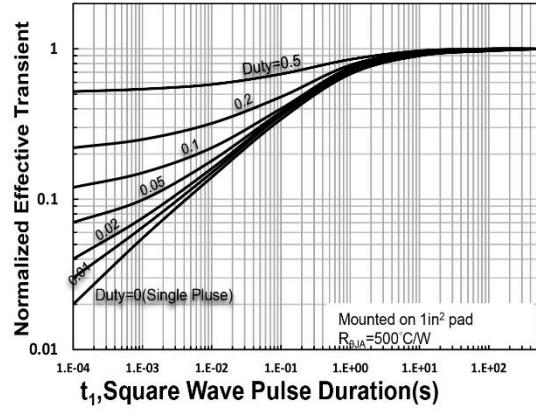


Figure 12. R_{QJA} Transient Thermal Impedance