Power MOSFETS

DATASHEET

LM60400DAK8A

Dual N-Channel

Enhancement Mode MOSFET

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Quality Management Systems

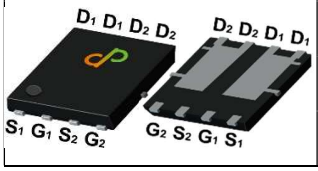
ISO 9001:2015 Certificate

LM60400DAK8A

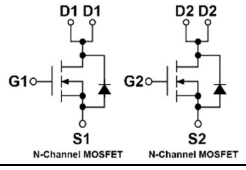
Dual N-Channel Enhancement Mode MOSFET

Pin Description

PDFN5*6(Dual) (TOP view)



Symbol



Product Summary

Symbol	Dual N-Channel	Unit
V_{DSS}	60	V
$R_{DS(ON)}$-Max	40	mΩ
ID	21.6	A

Feature

- Fast switching speed
- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- 100% UIS and Rg Tested

Applications

- Switching applications
- Battery Powered System

Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM60400DAK8A	PDFN5*6(Dual)	Tape & Reel	5000 / Tape & Reel	60400 □□□□□□

Note：□□□□□□ = Lot Code

Absolute Maximum Ratings (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter		Dual N-Channel	Unit
V_{DSS}	Drain-Source Voltage		60	V
V_{GSS}	Gate-Source Voltage		±20	
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature Range		-55 to 150	°C
I_S	Diode Continuous Forward Current	T_C=25°C	17	A
I_{DM}①	Pulse Drain Current Tested	T_C=25°C	54	A
I_D	Continuous Drain Current	T_C=25°C	21.6	A
		T_C=100°C	13.7	
P_D	Maximum Power Dissipation	T_C=25°C	18.7	W
		T_C=100°C	7.5	
I_D	Continuous Drain Current	T_A=25°C	6.0	A
		T_A=70°C	4.8	
P_D	Maximum Power Dissipation	T_A=25°C	1.4	W
		T_A=70°C	0.9	
I_{AS}②	Avalanche Current, Single pulse	L=0.1mH	16	A
		L=0.5mH	9	
E_{AS}②	Avalanche Energy, Single pulse	L=0.1mH	12.8	mJ
		L=0.5mH	20.3	

Thermal Characteristics

Symbol	Parameter		Rating	Unit
$R_{\theta JC}$	Thermal Resistance-Junction to Case	Steady State	6.7	°C/W
$R_{\theta JA}$③	Thermal Resistance-Junction to Ambient	Steady State	88	°C/W

Note ①：Max. current is limited by junction temperature.

Note ②：UIS tested and pulse width are limited by maximum junction temperature 150°C

Note ③：Surface Mounted on 1in^2 FR-4 board with 1oz.

Dual N-Channel Electrical Characteristics (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Electrical Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_{DS}=250uA	60	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=48V, V_{GS}=0V	-	-	1	uA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_{DS}=250uA	1.2	1.8	2.5	V
I_{GSS}	Gate Leakage Current	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
$R_{DS(ON)}$④	Drain-Source On-state Resistance	V_{GS}=10V, I_{DS}=10A	-	33	40	mΩ
		V_{GS}=4.5V, I_{DS}=5A	-	37	47	
gfs	Forward Transconductance	V_{DS}=5V, I_{DS}=10A	-	10	-	S
Dynamic Characteristics ⑤						
R_G	Gate Resistance	V_{GS}=0V,V_{DS}=0V, Freq.=1MHz	-	3.8	-	Ω
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=30V, Freq.=1MHz	-	1108	-	pF
C_{oss}	Output Capacitance		-	65	-	
C_{rss}	Reverse Transfer Capacitance		-	44	-	
$td_{(ON)}$	Turn-on Delay Time	V_{GS}=10V,V_{DS}=30V, I_D=1A,R_{GEN}=6Ω	-	6	-	nS
t_r	Turn-on Rise Time		-	21	-	
$t_{d(OFF)}$	Turn-off Delay Time		-	44	-	
t_f	Turn-off Fall Time		-	20	-	
Q_g	Total Gate Charge	V_{GS}=4.5V,V_{DS}=30V I_D=10A	-	13	-	nC
Q_g	Total Gate Charge	V_{GS}=10V,V_{DS}=30V, I_D=10A	-	26	-	
Q_{gs}	Gate-Source Charge		-	3.9	-	
Q_{gd}	Gate-Drain Charge		-	4.8	-	
Source-Drain Characteristics						
V_{SD}④	Diode Forward Voltage	I_{SD}=1A, V_{GS}=0V	-	0.7	1.1	V
t_{rr}	Reverse Recovery Time	I_F=4A, V_R=0V dI$_F$/dt=100A/μs	-	19.6	-	nS
Q_{rr}	Reverse Recovery Charge		-	15.1	-	nC

Note ④：Pulse test (pulse width≤300us, duty cycle≤2%).
Note ⑤：Guaranteed by design, not subject to production testing.

Dual N-Channel Typical Characteristics

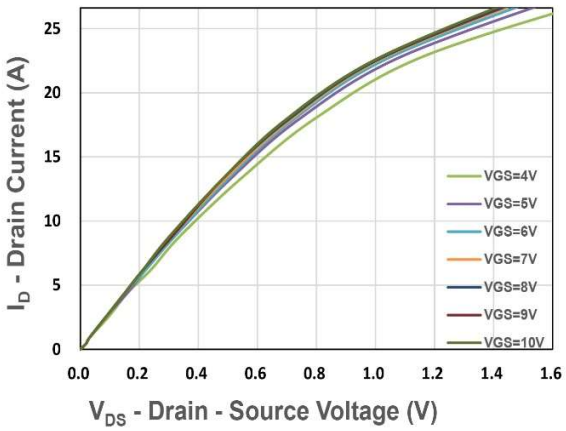


Figure 1. Output Characteristics

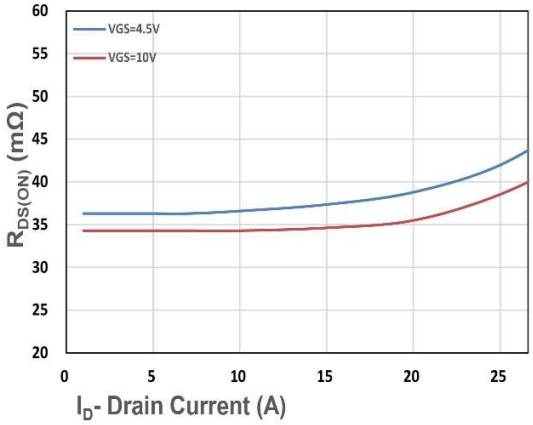


Figure 2. On-Resistance vs. ID

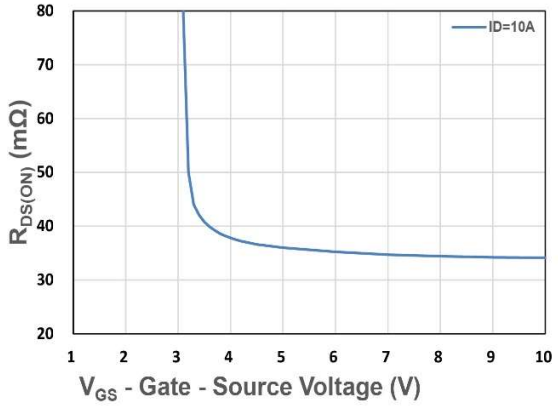


Figure 3. On-Resistance vs. VGS

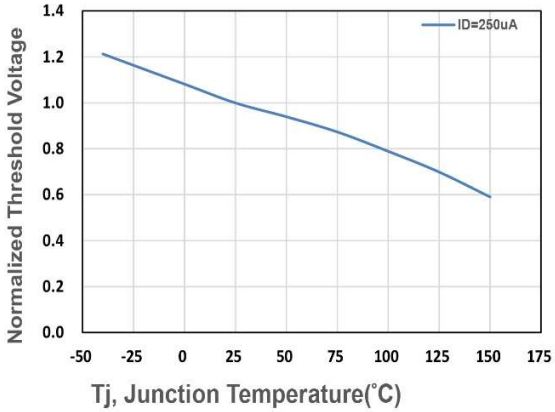


Figure 4. Gate Threshold Voltage

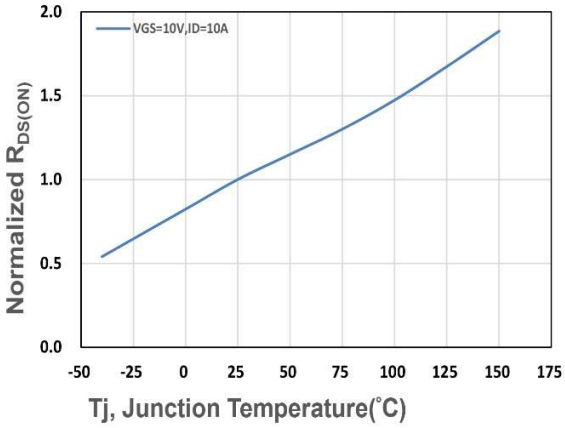


Figure 5. Drain-Source On Resistance

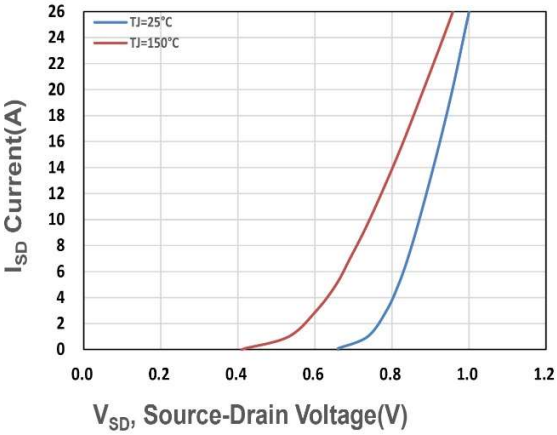


Figure 6. Source-Drain Diode Forward

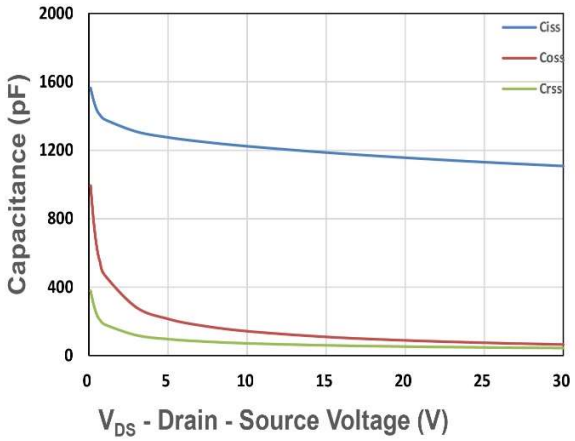


Figure 7. Capacitance

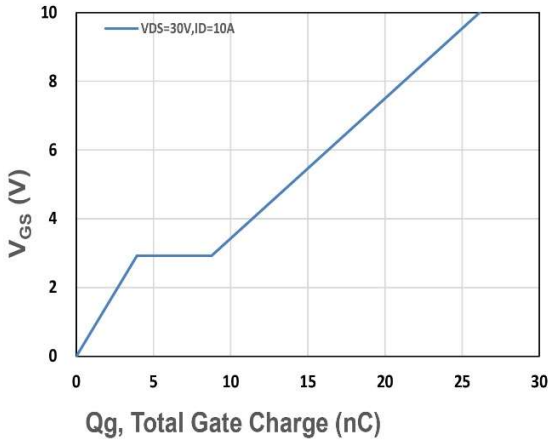


Figure 8. Gate Charge Characteristics

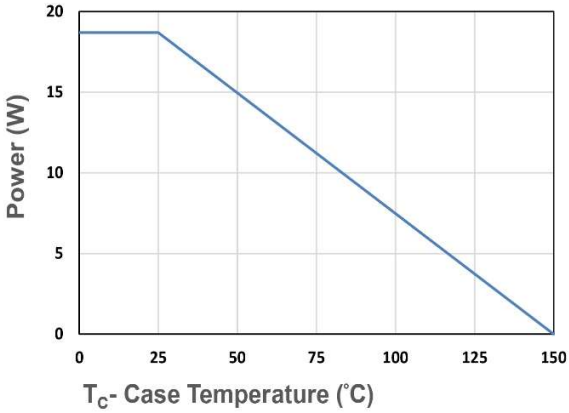


Figure 9. Power Dissipation

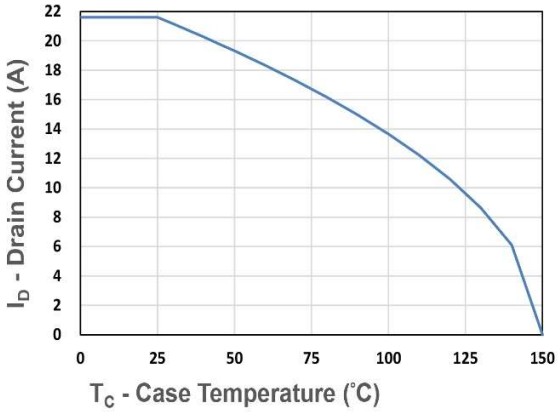


Figure 10. Drain Current

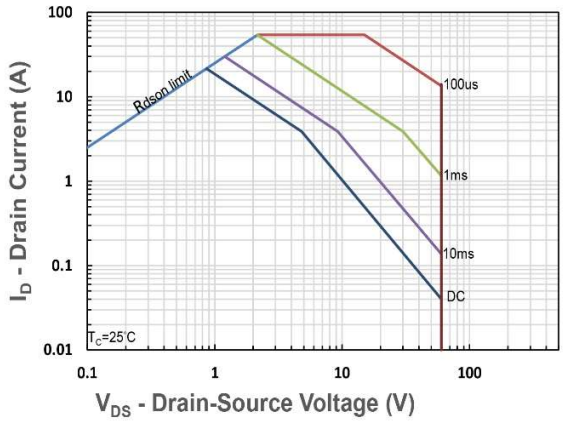


Figure 11. Safe Operating Area

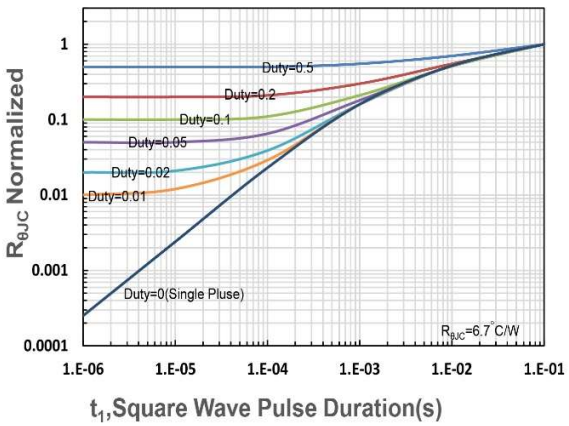


Figure 12. RθJC Transient Thermal Impedance