



Power MOSFETS

DATASHEET

LM7002KNEA3A

N-Channel
Enhancement Mode MOSFET

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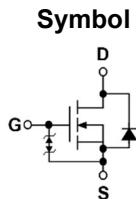
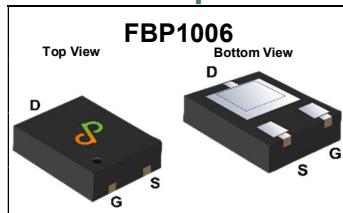


Quality Management Systems
ISO 9001:2015 Certificate

LM7002KNEA3A

N-Channel Enhancement Mode MOSFET

Pin Description



Ordering Information

Symbol	N-Channel	Unit
V_{DSS}	60	V
$R_{DS(ON)}\text{-Max}$	1.9	Ω
I_D	0.4	A

Feature

- Fast switching speed
- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- ESD Protection

Applications

- Small signal application
- Load switch

Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM7002KNEA3A	FBP1006	Tape & Reel	10000 / Tape & Reel	<input type="checkbox"/> 0

Note : = Lot Code

Absolute Maximum Ratings ($T_J=25^\circ\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	N-Channel	Unit
V_{DSS}	Drain-Source Voltage	60	V
V_{GSS}	Gate-Source Voltage	± 20	
T_J	Maximum Junction Temperature	150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$I_{DM}^{\text{(1)}}$	Pulse Drain Current Tested	$T_A=25^\circ\text{C}$	1.1
I_D	Continuous Drain Current	$T_A=25^\circ\text{C}$	0.4
		$T_A=70^\circ\text{C}$	0.3
P_D	Maximum Power Dissipation	$T_A=25^\circ\text{C}$	0.7
		$T_A=70^\circ\text{C}$	0.4

Thermal Characteristics

Symbol	Parameter	Rating	Unit
$R_{\theta JA}^{\text{(3)}}$	Thermal Resistance-Junction to Ambient	Steady State	180 $^\circ\text{C/W}$

Note ① : Max. current is limited by junction temperature.

Note ② : UIS tested and pulse width are limited by maximum junction temperature 150°C

Note ③ : Surface Mounted on 1in² FR-4 board with 1oz.

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N-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Electrical Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}$, $I_{\text{DS}}=250\mu\text{A}$	60	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{\text{DS}}=48\text{V}$, $V_{\text{GS}}=0\text{V}$	-	-	1	μA
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}$, $I_{\text{DS}}=250\mu\text{A}$	1	1.6	2.5	V
I_{GSS}	Gate Leakage Current	$V_{\text{GS}}=\pm 20\text{V}$, $V_{\text{DS}}=0\text{V}$	-	-	± 10	μA
$R_{\text{DS(ON)}}^{\circledast}$	Drain-Source On-state Resistance	$V_{\text{GS}}=10\text{V}$, $I_{\text{DS}}=0.3\text{A}$	-	1.6	1.9	Ω
		$V_{\text{GS}}=4.5\text{V}$, $I_{\text{DS}}=0.2\text{A}$	-	1.7	2.2	
g_{fs}	Forward Transconductance	$V_{\text{DS}}=10\text{V}$, $I_{\text{DS}}=0.2\text{A}$	-	0.45	-	S
Dynamic Characteristics [®]						
C_{iss}	Input Capacitance	$V_{\text{GS}}=0\text{V}$, $V_{\text{DS}}=30\text{V}$, Freq.=1MHz	-	26	-	pF
C_{oss}	Output Capacitance		-	2.7	-	
C_{rss}	Reverse Transfer Capacitance		-	1.7	-	
$t_{\text{d(ON)}}$	Turn-on Delay Time	$V_{\text{GS}}=10\text{V}$, $V_{\text{DS}}=30\text{V}$, $I_{\text{D}}=0.3\text{A}$, $R_{\text{GEN}}=10\Omega$	-	1	-	nS
t_{r}	Turn-on Rise Time		-	19.4	-	
$t_{\text{d(OFF)}}$	Turn-off Delay Time		-	23.2	-	
t_{f}	Turn-off Fall Time		-	21	-	
Q_{g}	Total Gate Charge	$V_{\text{GS}}=4.5\text{V}$, $V_{\text{DS}}=30\text{V}$ $I_{\text{D}}=1\text{A}$	-	0.9	-	nC
Q_{g}	Total Gate Charge	$V_{\text{GS}}=10\text{V}$, $V_{\text{DS}}=30\text{V}$, $I_{\text{D}}=1\text{A}$	-	1.7	-	
Q_{gs}	Gate-Source Charge		-	0.4	-	
Q_{gd}	Gate-Drain Charge		-	0.3	-	
Source-Drain Characteristics						
$V_{\text{SD}}^{\circledast}$	Diode Forward Voltage	$I_{\text{SD}}=0.2\text{A}$, $V_{\text{GS}}=0\text{V}$	-	0.8	1.1	V
t_{rr}	Reverse Recovery Time	$I_{\text{F}}=0.1\text{A}$, $V_{\text{R}}=10\text{V}$	-	7.4	-	nS
Q_{rr}	Reverse Recovery Charge	$dI_{\text{F}}/dt=100\text{A}/\mu\text{s}$	-	2.3	-	nC

Note ^④ : Pulse test (pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$).

Note ^⑤ : Guaranteed by design, not subject to production testing.

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N-Channel Typical Characteristics

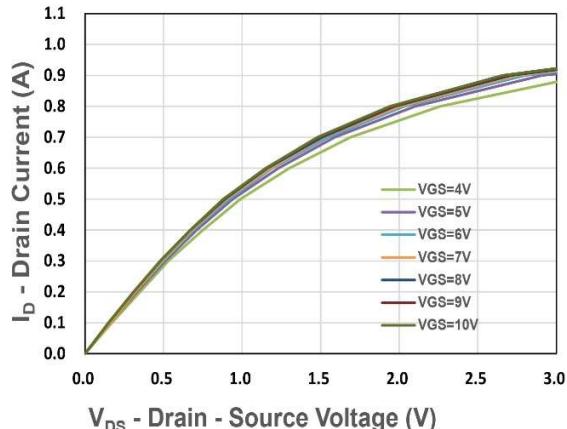


Figure 1. Output Characteristics

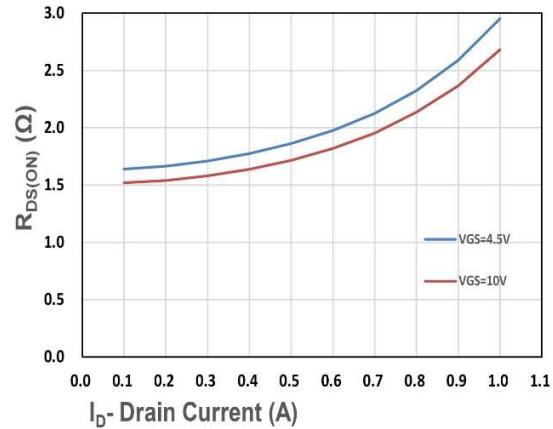


Figure 2. On-Resistance vs. ID

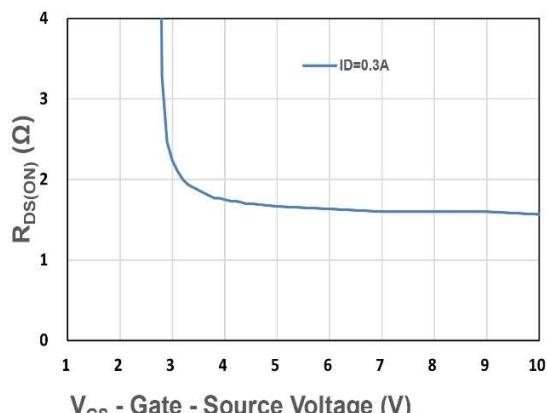


Figure 3. On-Resistance vs. VGS

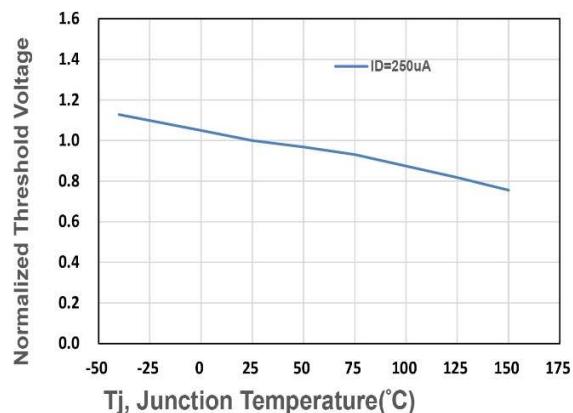


Figure 4. Gate Threshold Voltage

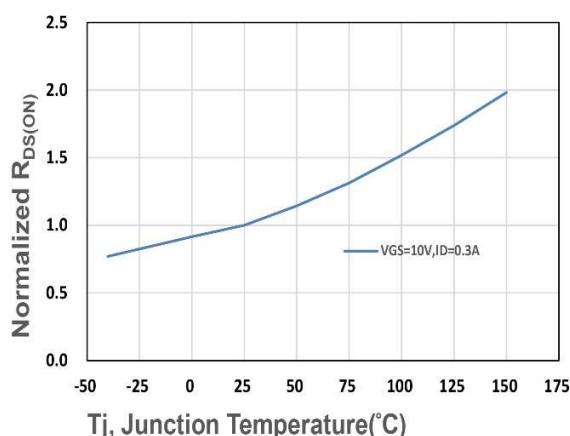


Figure 5. Drain-Source On Resistance

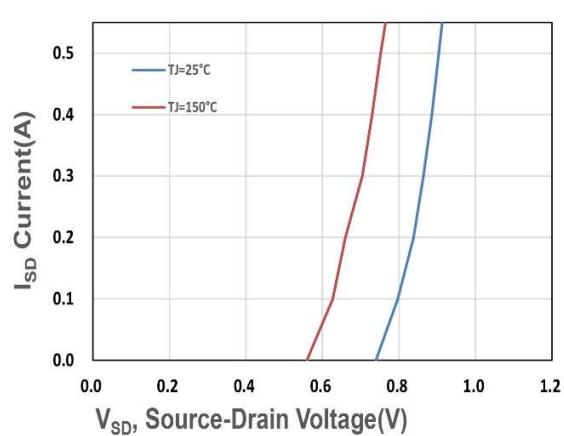


Figure 6. Source-Drain Diode Forward

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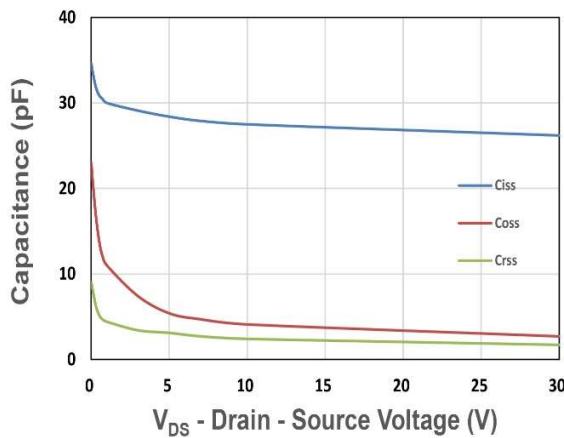


Figure 7. Capacitance

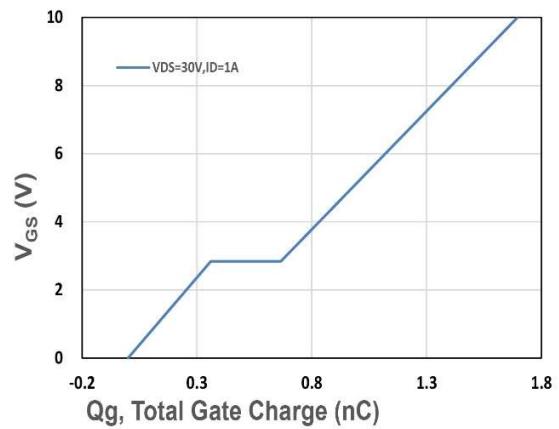


Figure 8. Gate Charge Characteristics

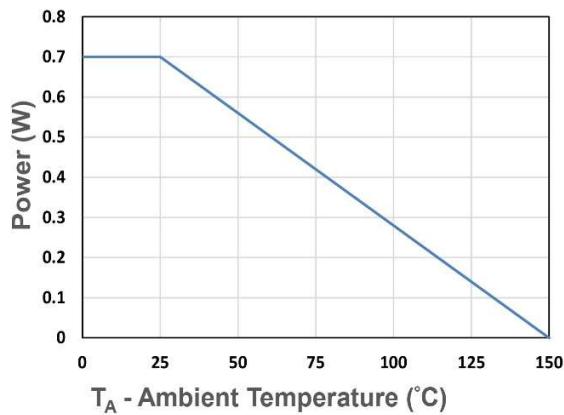


Figure 9. Power Dissipation

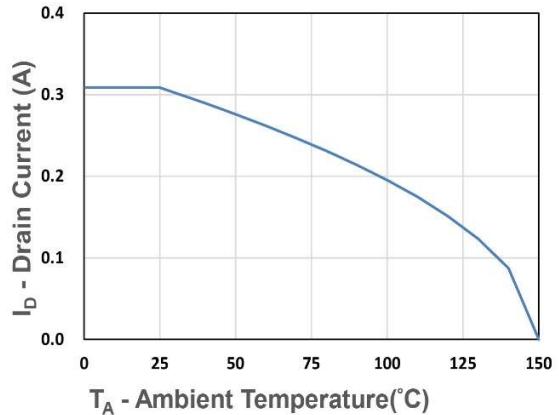


Figure 10. Drain Current

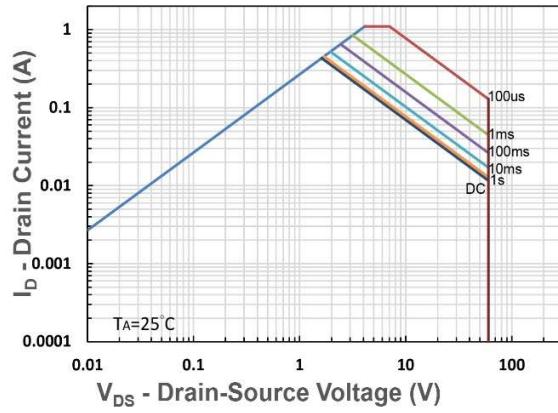


Figure 11. Safe Operating Area

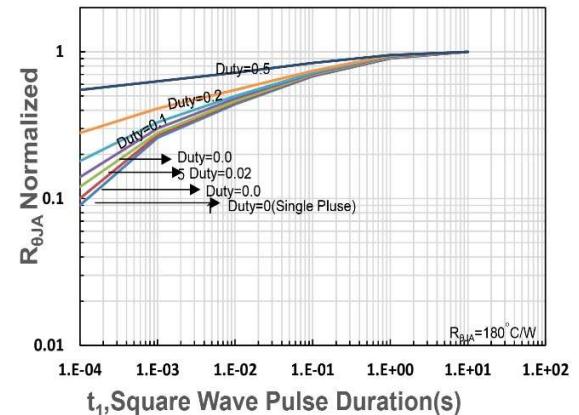


Figure 12. $R_{θJA}$ Transient Thermal Impedance