Power MOSFETS

DATASHEET

LM80012NHX8A

N-Channel

Enhancement Mode MOSFET

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Quality Management Systems

ISO 9001:2015 Certificate

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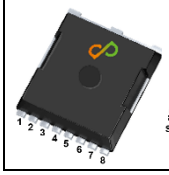
N-Channel Enhancement Mode MOSFET

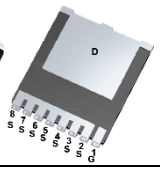
Pin Description

TOLL

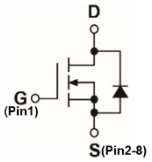
Top View



Bottom View



Symbol



Product Summary

Symbol	N-Channel	Unit
V_{DSS}	80	V
$R_{DS(ON)-Max}$	1.25	mΩ
ID	426	A

Feature

- Surface-mounted package
- Advanced trench cell design
- 100% UIS and Rg Tested

Applications

- Battery Management System
- Machine tool
- High power inverter system

Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM80012NHX8A	TOLL	Tape & Reel	2000 / Tape & Reel	80012 □□□□□□

Note：□□□□□□ = Lot Code

Absolute Maximum Ratings (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter		N-Channel	Unit
V_{DSS}	Drain-Source Voltage		80	V
V_{GSS}	Gate-Source Voltage		±20	
T_J	Maximum Junction Temperature		175	°C
T_{STG}	Storage Temperature Range		-55 to 175	°C
I_S	Diode Continuous Forward Current	T_C=25°C	113	A
I_{DM}	Pulse Drain Current Tested	T_C=25°C	1066	A
I_D①	Continuous Drain Current	T_C=25°C	426	A
		T_C=100°C	301	
P_D	Maximum Power Dissipation	T_C=25°C	375	W
		T_C=100°C	188	
I_D②	Continuous Drain Current	T_A=25°C	43	A
		T_A=70°C	36	
P_D②	Maximum Power Dissipation	T_A=25°C	3.8	W
		T_A=70°C	2.6	
I_{AS}③	Avalanche Current, Single pulse	L=0.1mH	100	A
		L=0.5mH	55	
E_{AS}③	Avalanche Energy, Single pulse	L=0.1mH	500	mJ
		L=0.5mH	756	

Thermal Characteristics

Symbol	Parameter		Rating	Unit
$R_{\theta JC}$	Thermal Resistance-Junction to Case	Steady State	0.4	°C/W
$R_{\theta JA}$②	Thermal Resistance-Junction to Ambient	Steady State	40	°C/W

Note ①：Max. current is limited by max. junction temperature.
Note ②： Surface Mounted on 1in^2 FR-4 board with 1oz
Note ③：UIS tested and pulse width are limited by maximum junction temperature 175°C

N-Channel Electrical Characteristics (T_J=25°C Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Electrical Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_{DS}=250uA	80	-	-	V
I_{DSS}	Drain Leakage Current	V_{DS}=64V, V_{GS}=0V	-	-	1	uA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_{DS}=250uA	2	-	4	V
I_{GSS}	Gate Leakage Current	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
$R_{DS(ON)}$④	Drain-Source On-state Resistance	V_{GS}=10V, I_{DS}=30A	-	1.0	1.25	mΩ
gfs	Forward Transconductance	V_{DS}=5V, I_{DS}=50A	-	87	-	S
Dynamic Characteristics ⑤						
R_G	Gate Resistance	V_{GS}=0V,V_{DS}=0V, Freq.=1MHz	-	0.7	-	Ω
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=40V, Freq.=1MHz	-	12230	-	pF
C_{oss}	Output Capacitance		-	3370	-	
C_{rss}	Reverse Transfer Capacitance		-	29	-	
$td_{(ON)}$	Turn-on Delay Time	V_{GEN}=10V,V_{DS}=40V, I_{DS}=1A,R_{GEN}=1Ω	-	44	-	nS
t_r	Turn-on Rise Time		-	27	-	
$t_{d(OFF)}$	Turn-off Delay Time		-	137	-	
t_f	Turn-off Fall Time		-	13	-	
Q_g	Total Gate Charge	V_{GS}=10V,V_{DS}=40V, I_D=30A	-	197	-	nC
Q_{gs}	Gate-Source Charge		-	61	-	
Q_{gd}	Gate-Drain Charge		-	47	-	
Source-Drain Characteristics						
V_{SD}④	Diode Forward Voltage	I_{SD}=30A, V_{GS}=0V	-	0.75	1.1	V
t_{rr}	Reverse Recovery Time	I_{DS}=15A, V_{GS}=0V dI$_{SD}$/dt=100A/μs	-	27	-	nS
Q_{rr}	Reverse Recovery Charge		-	34	-	nC

Note ④：Pulse test (pulse width≤300us, duty cycle≤2%).
Note ⑤：Guaranteed by design, not subject to production testing.

N-Channel Typical Characteristics

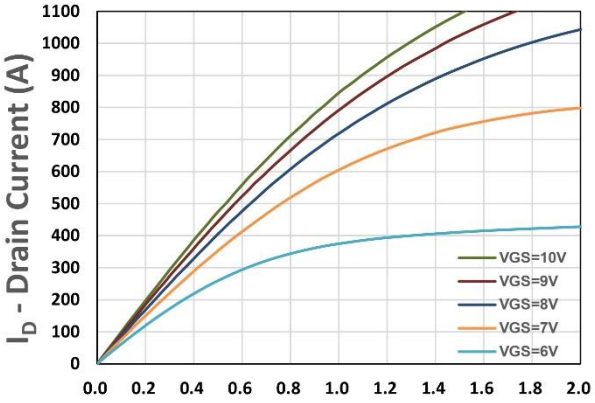


Figure 1. Output Characteristics

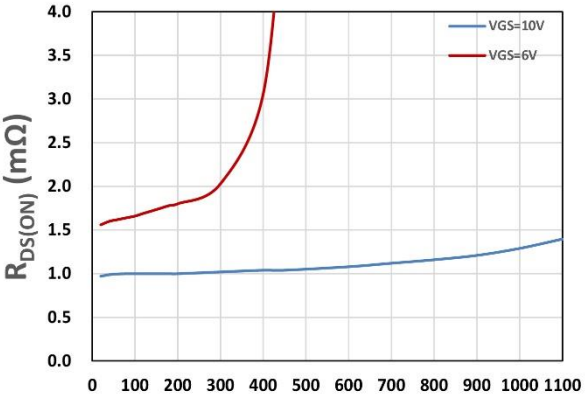


Figure 2. On-Resistance vs. ID

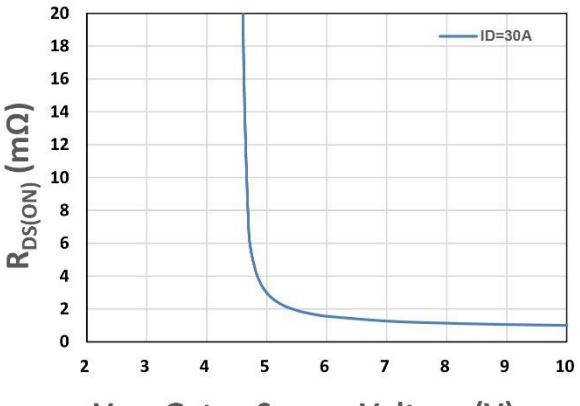


Figure 3. On-Resistance vs. VGS

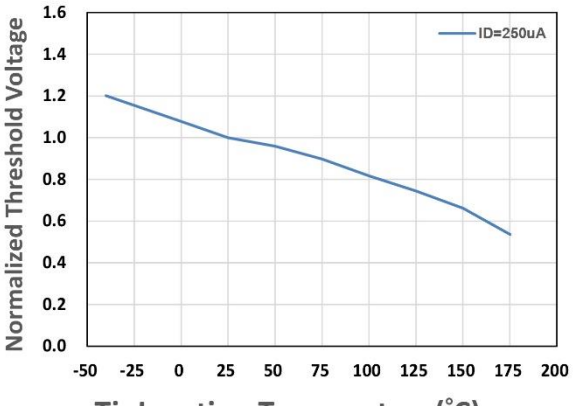


Figure 4. Gate Threshold Voltage

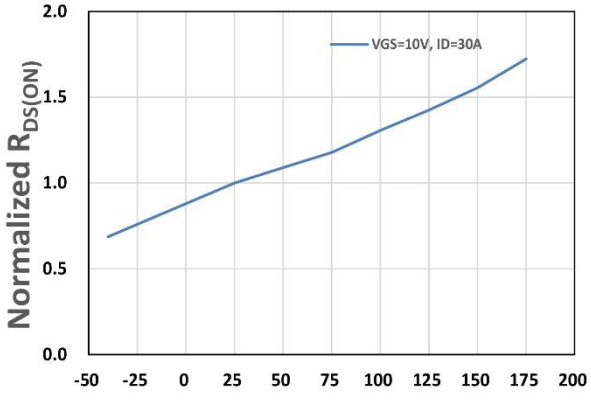


Figure 5. Drain-Source On Resistance

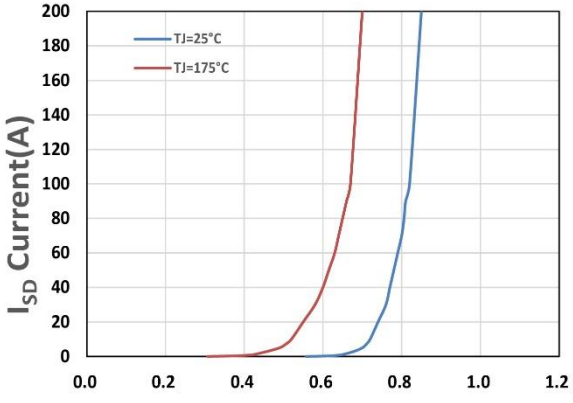


Figure 6. Source-Drain Diode Forward

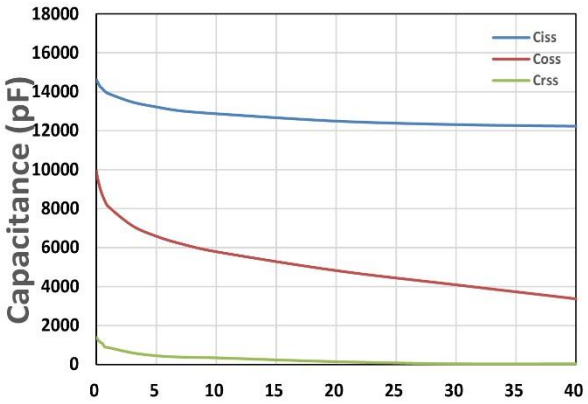


Figure 7. Capacitance

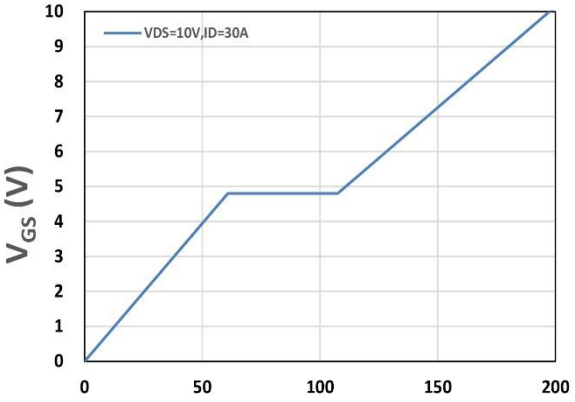


Figure 8. Gate Charge Characteristics

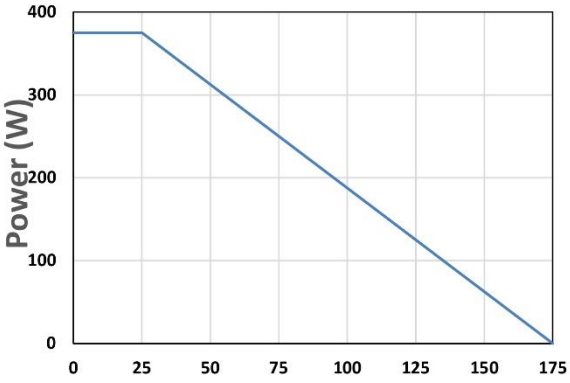


Figure 9. Power Dissipation

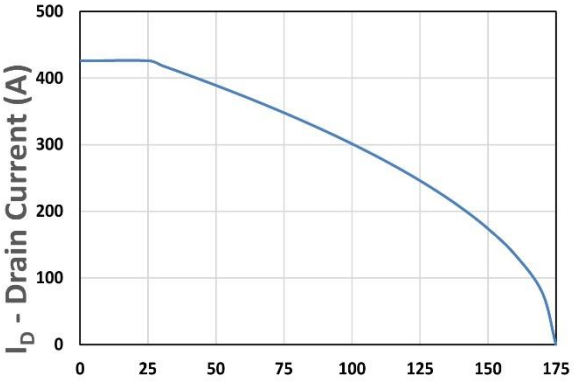


Figure 10. Drain Current

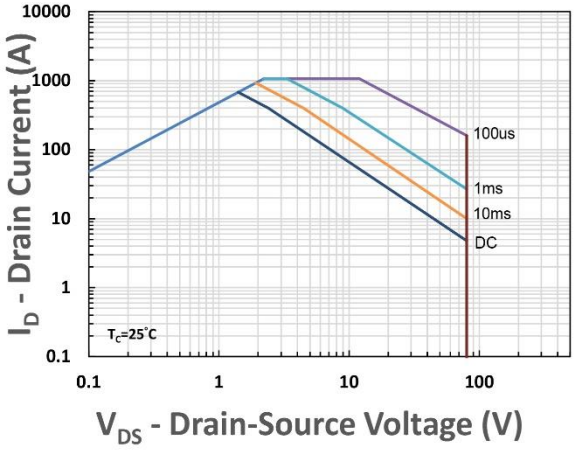


Figure 11. Safe Operating Area

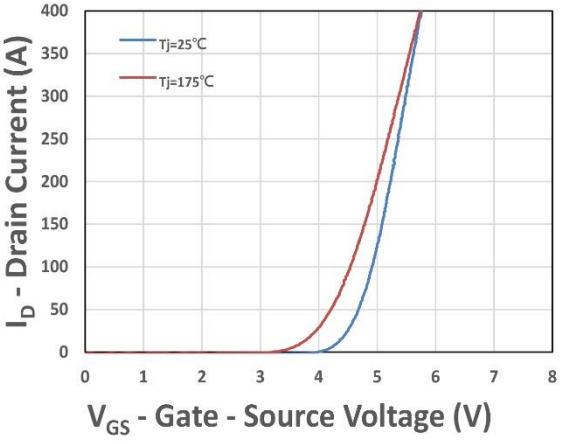


Figure 12. Transfer Characteristics

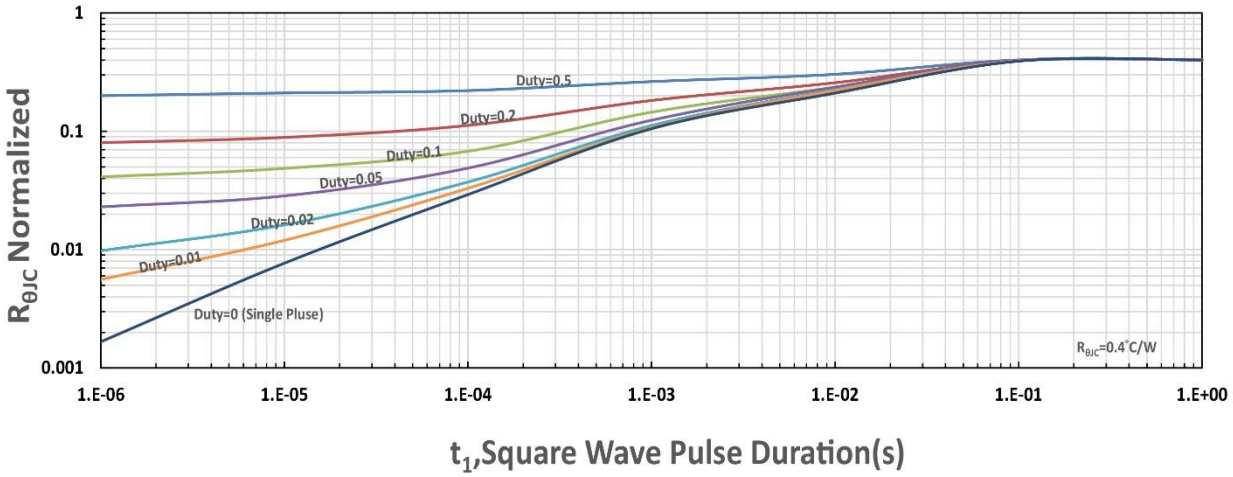


Figure 13. RθJC Transient Thermal Impedance