



Power MOSFETS

DATASHEET

LM25006NAM8A

N-Channel
Enhancement Mode MOSFET

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Quality Management Systems
ISO 9001:2015 Certificate

N-Channel Enhancement Mode MOSFET

Pin Description

LFPAK56		Symbol	Symbol	N-Channel	Unit
Top view	Bottom view			V _{DSS}	V
				R _{DSON-Max}	mΩ
				I _D	A

Feature

- Reliable and Rugged
- ROHS Compliant & Halogen-Free
- 100% UIS and Rg Tested

Product Summary

Applications

- Power Load Switch
- O ring FETs

Ordering Information

Orderable Part Number	Package Type	Form	Shipping	Marking
LM25006NAM8A	LFPAK56	Tape & Reel	4000 / Tape & Reel	25006

Note: = Lot code

Absolute Maximum Ratings (TJ=25°C Unless Otherwise Noted)

Symbol	Parameter	N-Channel	Unit
V _{DSS}	Drain-Source Voltage	25	V
V _{GSS}	Gate-Source Voltage	±16	
T _J	Maximum Junction Temperature	175	°C
T _{STG}	Storage Temperature Range	-55 to 175	°C
I _S	Diode Continuous Forward Current	T _c =25°C 57	A
I _{DM} ^①	Pulse Drain Current Tested	T _c =25°C 1023	A
I _D	Continuous Drain Current	T _c =25°C 400	A
		T _c =100°C 289	
P _D	Maximum Power Dissipation	T _c =25°C 125	W
		T _c =100°C 63	
I _D ^②	Continuous Drain Current	T _A =25°C 67	A
		T _A =70°C 56	
P _D ^②	Maximum Power Dissipation	T _A =25°C 3.2	W
		T _A =70°C 2.3	
I _{AS} ^③	Avalanche Current, Single pulse	L=0.1mH 86	A
E _{AS} ^③	Avalanche Energy, Single pulse	L=0.1mH 369	mJ
I _{AS} ^③	Avalanche Current, Single pulse	L=0.5mH 49	A
E _{AS} ^③	Avalanche Energy, Single pulse	L=0.5mH 597	mJ

Thermal Characteristics

Symbol	Parameter	Rating	Unit
R _{θJC}	Thermal Resistance-Junction to Case	Steady State 1.2	°C/W
R _{θJA} ^②	Thermal Resistance-Junction to Ambient	Steady State 45	°C/W

Note ① : Max. current is limited by junction temperature.

Note ② : Surface Mounted on 1in² FR-4 board with 1oz.

Note ③ : UIS tested and pulse width are limited by maximum junction temperature 175°C.

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N-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Electrical Characteristics						
$\mathbf{BV_{DSS}}$	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}, I_{DS}=250\mu\text{A}$	25	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=20\text{V}, V_{GS}=0\text{V}$	-	-	1	μA
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_{DS}=250\mu\text{A}$	1	1.4	1.9	V
I_{GSS}	Gate Leakage Current	$V_{GS}=\pm 16\text{V}, V_{DS}=0\text{V}$	-	-	± 100	nA
$R_{DS(\text{ON})}^{\text{(4)}}$	Drain-Source On-state Resistance	$V_{GS}=10\text{V}, I_{DS}=20\text{A}$	-	0.38	0.57	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}, I_{DS}=10\text{A}$	-	0.57	0.81	
g_{fs}	Forward Transconductance	$V_{DS}=5\text{V}, I_{DS}=10\text{A}$	-	71	-	S
Dynamic Characteristics ⁽⁵⁾						
R_G	Gate Resistance	$V_{GS}=0\text{V}, V_{DS}=0\text{V},$ Freq.=1MHz	-	1.3	-	Ω
C_{iss}	Input Capacitance	$V_{GS}=0\text{V},$ $V_{DS}=12.5\text{V},$ Freq.=1MHz	-	10670	-	pF
C_{oss}	Output Capacitance		-	5305	-	
C_{rss}	Reverse Transfer Capacitance		-	3682	-	
$t_{d(\text{ON})}$	Turn-on Delay Time	$V_{GS}=10\text{V}, V_{DS}=12.5\text{V},$ $I_D=1\text{A}, R_{GEN}=1\Omega$	-	18	-	nS
t_r	Turn-on Rise Time		-	27	-	
$t_{d(\text{OFF})}$	Turn-off Delay Time		-	97	-	
t_f	Turn-off Fall Time		-	74	-	
Q_g	Total Gate Charge	$V_{GS}=4.5\text{V}, V_{DS}=12.5\text{V}$ $I_D=20\text{A}$	-	151	-	nC
Q_g	Total Gate Charge	$V_{GS}=10\text{V}, V_{DS}=12.5\text{V},$ $I_D=20\text{A}$	-	248	-	
Q_{gs}	Gate-Source Charge		-	23	-	
Q_{gd}	Gate-Drain Charge		-	88	-	
Source-Drain Characteristics						
$V_{SD}^{\text{(4)}}$	Diode Forward Voltage	$I_{SD}=10\text{A}, V_{GS}=0\text{V}$	-	0.69	1.1	V
t_{rr}	Reverse Recovery Time	$I_F=10\text{A}, V_R=12.5\text{V}$ $dI_F/dt=100\text{A}/\mu\text{s}$	-	82	-	nS
Q_{rr}	Reverse Recovery Charge		-	62	-	nC

Note ⁽⁴⁾ : Pulse test (pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$).

Note ⁽⁵⁾ : Guaranteed by design, not subject to production testing.

N-Channel Typical Characteristics

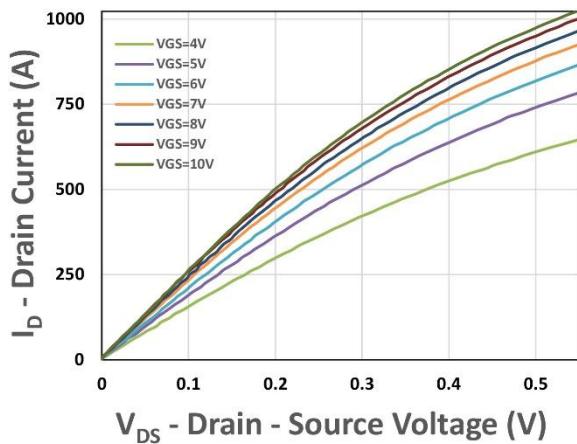


Figure 1. Output Characteristics

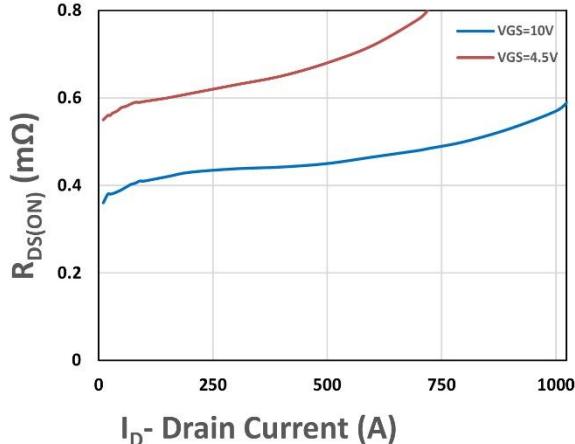


Figure 2. On-Resistance vs. ID

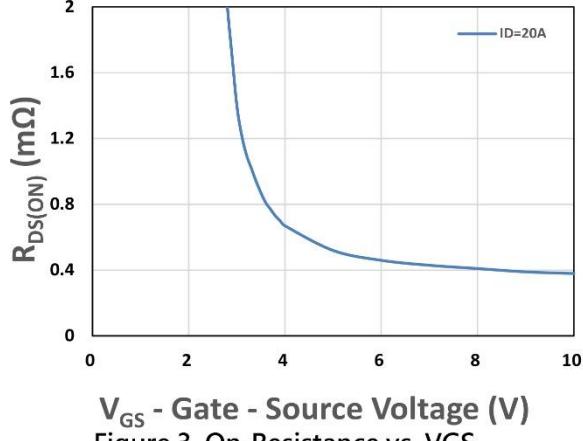


Figure 3. On-Resistance vs. VGS

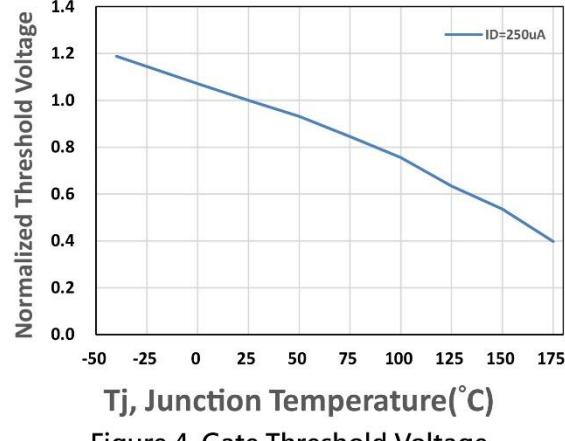


Figure 4. Gate Threshold Voltage

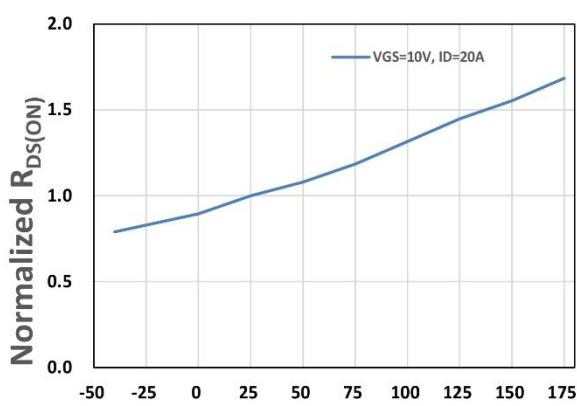


Figure 5. Drain-Source On Resistance

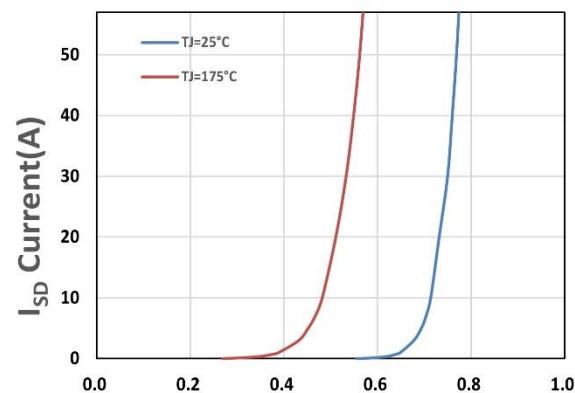
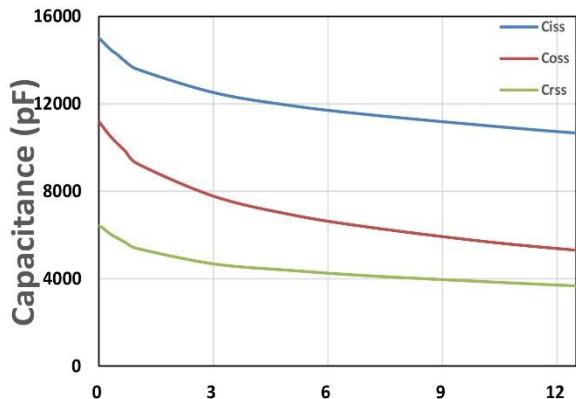
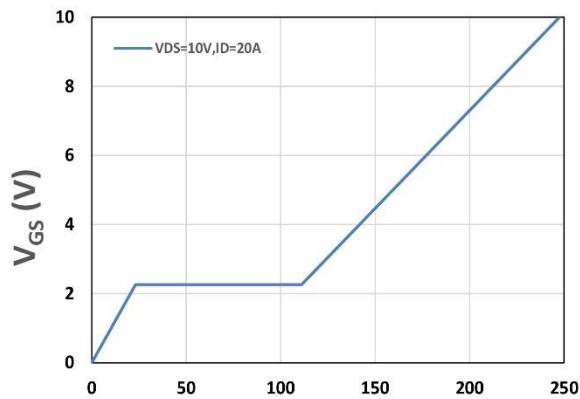


Figure 6. Source-Drain Diode Forward

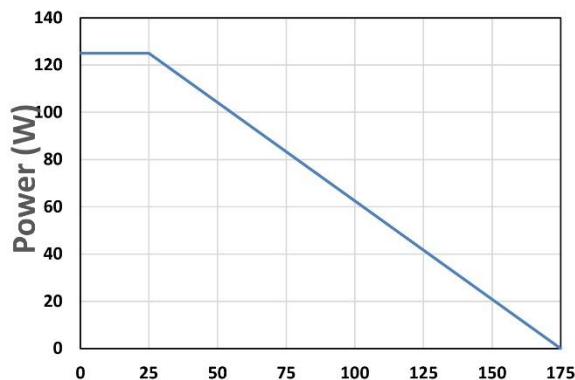
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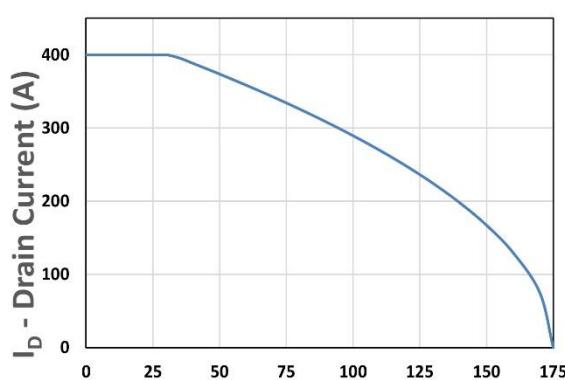
V_{DS} - Drain - Source Voltage (V)
Figure 7. Capacitance



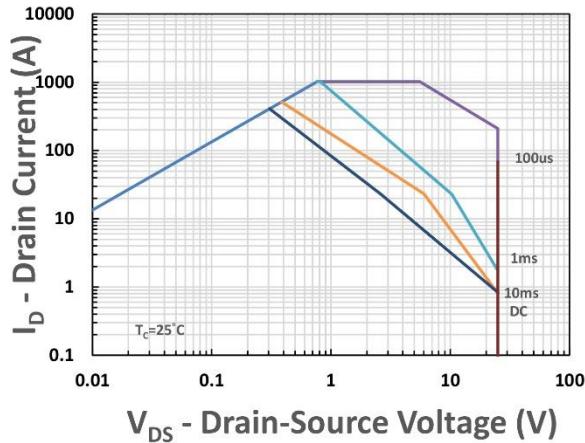
Q_g , Total Gate Charge (nC)
Figure 8. Gate Charge Characteristics



T_c -Case Temperature (°C)
Figure 9. Power Dissipation

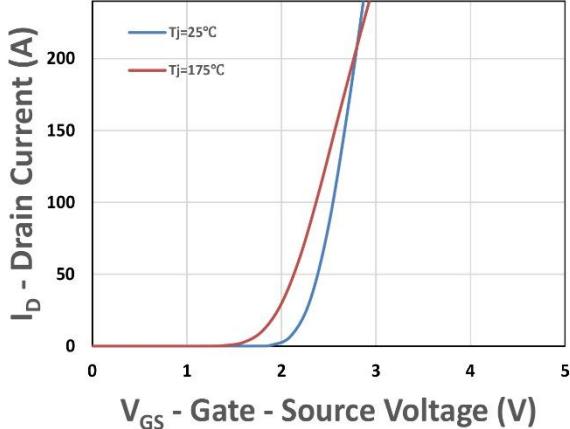


T_c -Case Temperature (°C)
Figure 10. Drain Current



V_{DS} - Drain-Source Voltage (V)

Figure 11. Safe Operating Area



V_{GS} - Gate - Source Voltage (V)

Figure 12. Transfer Characteristics

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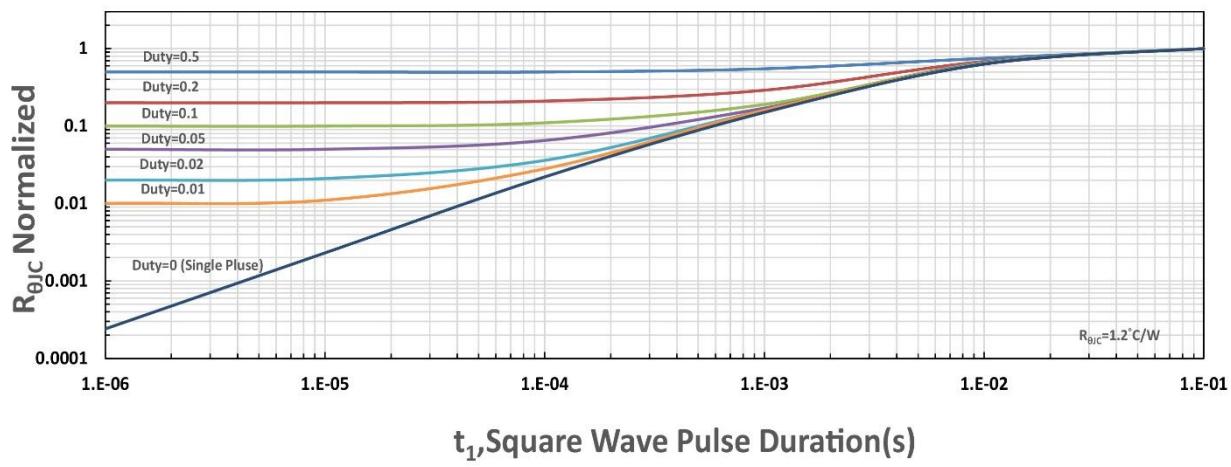


Figure 13. $R_{\theta JC}$ Transient Thermal Impedance